Tracking the Formation of a Break Junction Formed by Electromigration using Transmission Electron Microscopy

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ABSTRACT

Nanogaps formed by electromigration of metal nanowires have been widely employed as platforms to study electrical conduction through single molecules and atom clusters. In this research, we investigated the nanogap formation in gold nanowires through electromigration using transmission electron microscopy (TEM). In order to do so, we patterned nanowires on a silicon nitride TEM membrane using electron beam lithography (EBL) followed by gold deposition and liftoff. We thinned these nanowires slowly through a controlled passage of current. Our results indicated that the crystals in the gold nanowires fused into larger grains during the electromigration. Further passage of current caused nanowire to form a ~3nm wide neck region which eventually breaks to form a nanogap. Thus resultant tips flanking the nanogap tended to have atomic scale sharpness, which allows the precise position of objects of interest.
Key words: Transmission electron microscopy, nanowires, nanogaps, molecular electronics, electromigration.

1. INTRODUCTION

The continuous trend of miniaturization in microelectronics industry will eventually lead to the device made of single molecule or atom clusters. Recently, a single electron transistor (SET) made of a single gold nanocrystal captured between a pair of gold electrodes has been realized[1]. Double stranded deoxynucleic acid (DNA) oligonucleotides covalently bridging gold electrodes were found to exhibit a nonlinear conduction behavior[2]. In both of these exciting research works, nanogaps formed through electromigration, or so-called break junctions were used to connect the entities of interest into the circuitry. More interestingly, the break junctions themselves revealed quantum conduction behaviors such as Kondo effects[3] and Coloumb blockade[4, 5] during their formation. Even though these devices based on the break junctions have produced insightful and exciting results, the yield of these devices remains poor. To increase the yield so that large-scale fabrication of molecular devices can be possible, a more thorough understanding on the evolution of the junction breaking is needed.

In this paper, we fabricated gold break junctions on a transmission electron microscopy silicon nitride membrane and broke these junctions to form nanogaps using electromigration in a highly controllable fashion with an elaborated voltage ramping algorithm. We used transmission electron microscopy (TEM) to track the formation of the nanogap. We obtained images of the break junctions with resolutions much better than scanning electron microscopy (SEM) and most importantly we were able to view the morphological transitions of the break junctions, which are unobservable by SEM. Our results also indicated that these break junctions have extremely sharp tips, which could help single molecule to transverse the nanogap.

2. FABRICATION OF THE BREAK JUNCTIONS ON TEM SILICON NITRIDE MEMBRANE

The substrate on which the break junctions are patterned is a special TEM membrane manufactured by Structure Probe Inc. (West Chester, PA). This 100 nm thick silicon nitride membrane is supported on a 200 µm thick and 3 mm × 3 mm wide silicon chip. Silicon substrate at the center of the chip is completely removed by an anisotropic etch so a freestanding 0.5 mm × 0.5 mm silicon nitride membrane window is formed. The schematic of the grid is shown in Figure 1.

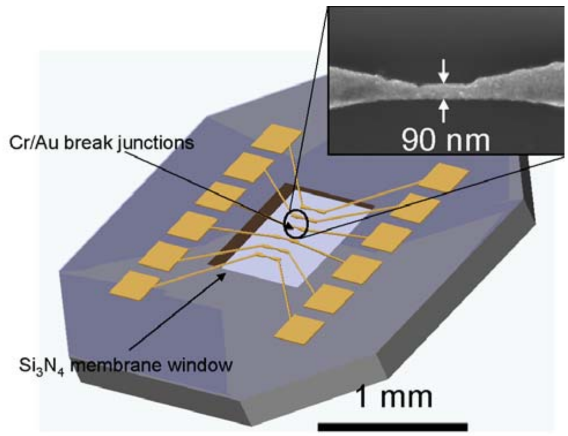

Figure 1. Schematic showing the TEM silicon nitride membrane patterned with six break junctions, their leads and contact pads. The inset shows an SEM image of one of the Nanowires.

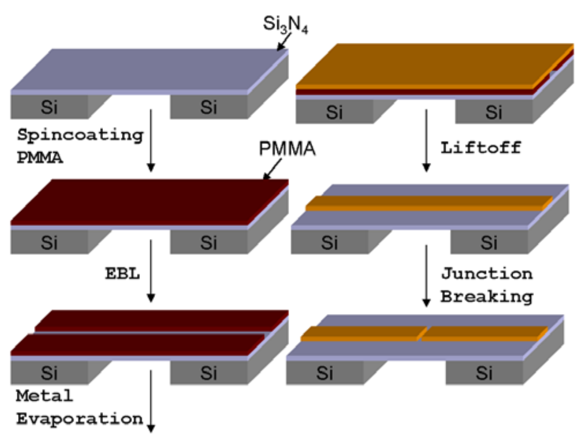

Figure 2. Schematic showing the patterning process of the break junctions.

To ease the handling of a chip with such a small size during the break junction patterning, we glued it on a 1 cm × 1 cm silicon wafer with a piece of conductive tape. Then we spincoated a 150 nm thick polymethylmethacrylate (PMMA) on the chip at 2,500 rpm followed by 90 second prebaking at

180°C. We performed electron beam lithography (EBL) to pattern an array of six junctions, their connecting leads and contact pads on the chip. After the completion of EBL, we postbaked the chip at 95°C for 30 minutes. Then we evaporated 2 nm thick Cr and 35 nm thick Au on the chip and soaked the chip in acetone for 9 hrs for liftoff. The schematic illustrating the fabrication process is shown in Figure 2.

3. TEM Studies on the Nanowires Undergoing Electromigration

The electromigration experiments were performed by applying voltage provided by a Keithley 6430 remote sourcemeter (Keithley Instruments Inc., Cleveland, OH) associated with a DesertCryogenics probe station (Desert Cryogenics, Tucson, AZ) on the contact pads connected to two terminals of the break junction. The voltage ramping software was written using Labview 6.0 program (National Instruments Corp., Austin, TX). The algorithm is shown in Figure 3 and described below.

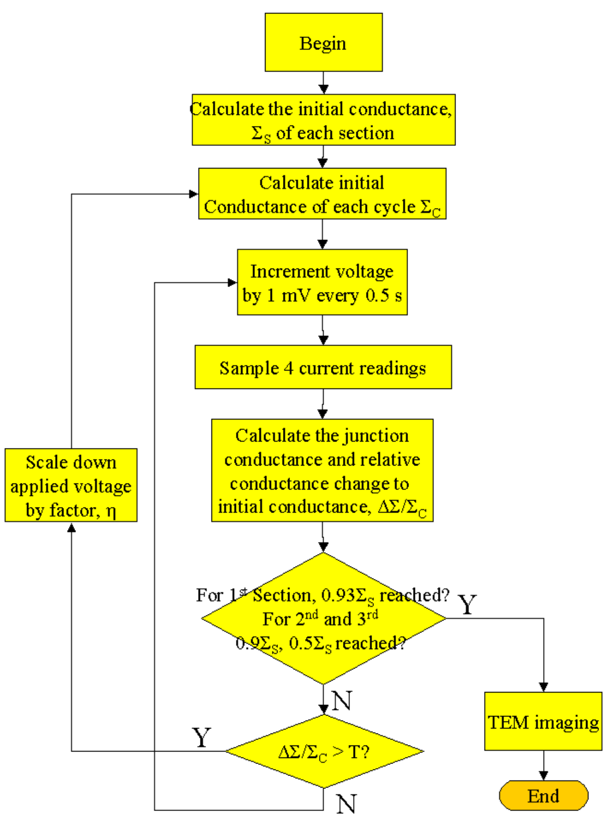

Figure 3. Flow chart showing the controlled voltage ramp-up algorithm.

The electromigration experiment can be divided into three voltage ramp-up sections. At the beginning of each section, voltage applied across the junction was initially ramped up from 1 mV and the initial conductance was recorded as Σ_S. Each section itself is comprised of multiple voltage ramp-up cycles. In each cycle, the voltage applied across the break junction was incremented 1 mV every 0.5 second. During this half-second dwelling time, four current samplings were carried out. Average of these four current readings was then divided by the applied voltage to give a near real-time junction conductance, Σ_R. At the beginning of each voltage ramp up cycle, the initial conductance of the break junction, Σ_C will be recorded and relative change from Σ_C by Σ_R is calculated and compared to a threshold T. Once this relative change is larger than T, the applied bias will be scaled down by a ratio, η and another cycle of ramp up will be started with ηV as the initial voltage. Through this method, the voltage is controlled by the junction conductance change via a negative feedback loop. The parameters T and η determine the correlation between the voltage and conductance change.

During the first section of junction breaking, the values of T and η were set to be 0.01 and 0.95, respectively. When the relative change from Σ_S by the near real-time conductance is larger than 7%, this section would be terminated and TEM images were taken. For the following sections, we changed relative conductance change threshold, T to 0.005, which made the electromigration process slower. Second section would be terminated when $0.9\Sigma_S$ was reached and third section was terminated when $0.5\ \Sigma_S$ was reached.

TEM images of the break junctions were taken with a Philips EM420T transmission electron microscope (Hillsboro, OR). The high tension voltage during the imaging process was set to be 120 KeV. After the images were taken, the films were developed and digital images were scanned using a scanner.

4. Results and Discussions

The break junction after the fabrication has a center wire with a 200 nm length and 90 nm width. At the ends of the center wire, a 1 µm wide lead are tapered to 90 nm center wire in 3 µm distance. The other end of the lead was connected to a 250 µm × 200 µm contacting pad located on the Si substrate via a 10 µm wide gold wire.

Figure 4 shows the current/voltage curves of three sections and Figure 5 shows the TEM images taken after each section showing the evolution of a break junction. By comparing the TEM images of the break junction before and after the first voltage ramp-up section, we observed a reorganization of gold polycrystalline grains. The gold grain size tends to be much larger after the passage of the current, which suggested the occurrence of the fusion of the small grains. Considering the cross sectional area of the center nanowire is 3.15×10^{-15} m^2, current density through the center nanowires can be as high as 7×10^{11} A/m^2. Therefore, such an enormous current density could easily brought up the temperature of the junction by Joule heating and resulted in the fusion of gold crystalline grains[6].

These TEM images also indicated that thinning of the nanowires by the electromigration was not uniform. Large grains of the gold wire were removed completely after the first voltage ramp-up section. The loss of a whole grain tended to cause the formation of a neck region. Figure 4 shows that the width of the neck region can be as narrow as 3~5 nm, which is comprised of 10~17 gold atoms considering an Au lattice constant of 2.884 Å[7]. Further passage of current led to the junction breaking at this narrow neck region to make a nanogap flanked by extremely sharp tips. Tips with such a small dimension reduced the possibility of connecting multiple molecules or atom clusters across the break junction, hence the electrical behavior of single molecule can be studied.

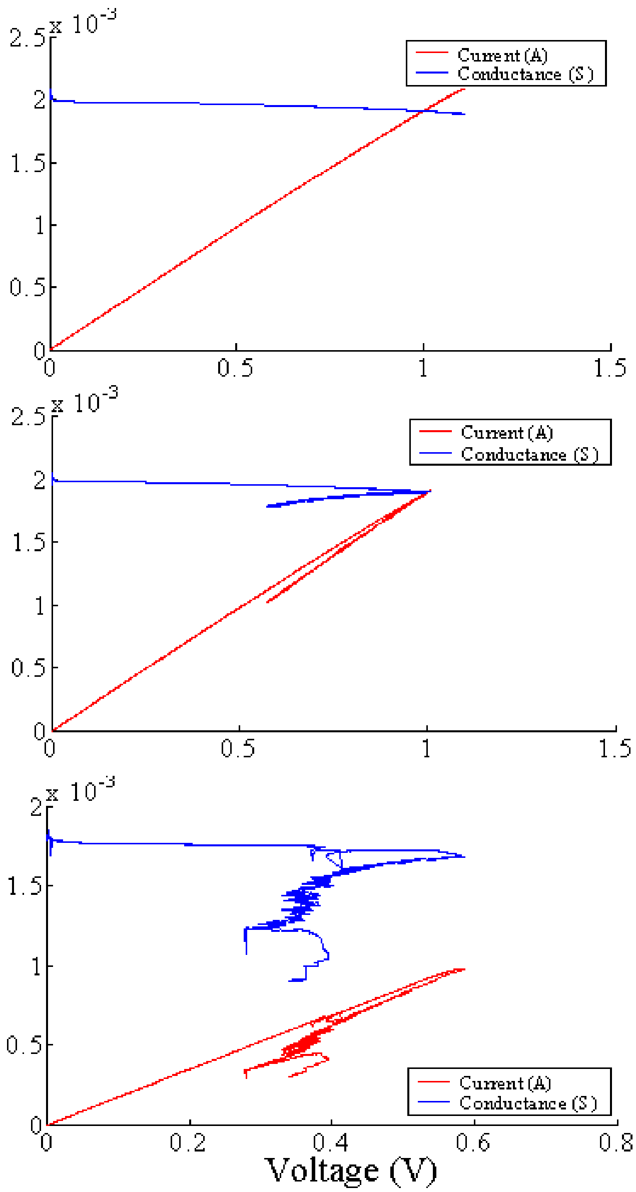

Figure 4. I/V curves of a break junction after each voltage ramp-up section and their associated.

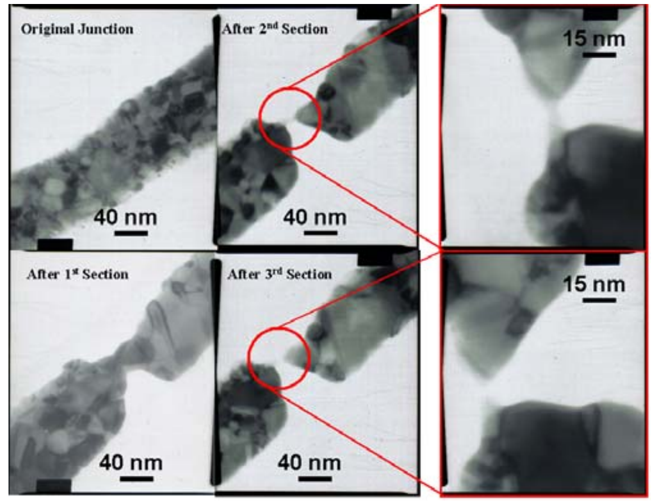

Figure 5. TEM images showing the evolution of the junction breaking in Figure 4.

In summary, we have successfully fabricated break junctions on a TEM nitride membrane grid and for the first time tracked the formation of break junction using TEM. With an elaborately designed voltage ramp-up algorithm, we have performed a slow thus highly controllable junction breaking. During this process, we observed crystal reorganization that is likely to be caused by Joule heating due to a passage of high density current. One unique feature of our break junction distinguishing our break junctions from those fabricated by other researchers is its sharp tip flanking the nanogap. These sharp tips minimize the linkage of multiple molecules across the junction, therefore electrical behavior of single molecule instead of an averaged behavior of multiple molecules could be studied.

5. ACKNOWLEDGEMENT

We would like to thank the staff of the Nanotechnology User Facility at the University of Washington for their assistance in electron beam lithography. We are also indebted to Dr. Thomas Murray at the Material Sciences and Engineering Department at the University of Washington for his help in TEM. JD thanks the Nanotechnology Fellowship sponsored by the University Initiative Fund (UIF). The research was supported in part by the Center of Excellence in Genomic Sciences at the University of Washington.

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