BSIM4 and BSIM Multi-Gate Progress

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ABSTRACT

New technologies and alternate transistor structures are being developed to extend the CMOS scaling. Device models need to be developed and improved in parallel with the technology advancements to enable an efficient and quick adoption of the new technologies. Some of the recent advances in BSIM4 and BSIM Multi-gate models towards meeting this goal are presented in this paper. Improvements to the BSIM4 model include holistic stress-induced mobility enhancement model and a high-k dynamic behavior model. Preliminary results of the modeling of multi-gate architectures are also presented.

Keywords: MOSFET modeling, BSIM, process-induced strain, high-k dielectrics, double-gate MOSFETs.

1 INTRODUCTION

The semiconductor industry is facing technological challenges to maintain the constant bulk CMOS scaling. To meet the challenge, the industry has started introducing new materials into bulk CMOS and developing new device structures [1]. Efforts towards modeling of the associated new device behavior are presented in this paper. Mobilities of both carriers - electrons and holes, can be enhanced by introducing stress into the inversion layer through addition of new materials into the CMOS process [2], [3]. A layout dependent, holistic model for mobility enhancement through process-induced stress is developed [4]. High-k dielectrics use larger physical thickness for the same EOT thereby reducing gate tunneling current and enabling bulk CMOS scaling [5]. The dynamic behavior introduced into the transistor operation by the use of high-k dielectrics is modeled and can be incorporated into BSIM4 through a simple sub-circuit [6]. Multi-gate transistors have a strong potential to extend CMOS scaling into sub-25nm regime [7]. A preview of DG-MOSFET modeling is presented. Comparisons of the model with 2-D simulator are shown for symmetric DG-MOSFET with finite body doping [8].

2 MOBILITY MODEL FOR PROCESS-INDUCED STRESS

Application of stress changes the resistivity of silicon [9]. Stress can be introduced into inversion channel in many ways, ex. STI, SiGe S/D. Mobility enhancement of carriers is proportional to the average stress in the channel, S_{AVG}.

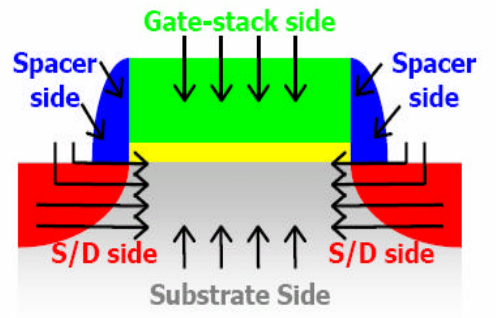

Figure 1: The four distinct directions of stress transfer.

$$\frac{\Delta m}{m} \propto S_{AVG} \tag{1}$$

Stress is transferred to the channel from four distinct directions as shown in Fig. 1. The substrate side stress is modeled simply by a constant since it is nearly layout independent. Stress models are developed for the other stress transfer directions and combined to produce the complete layout-dependent holistic mobility model.

S/D side stress can originate due a stressor inside the S/D (ex. SiGe S/D) or adjacent to the S/D (ex. STI) or on top of S/D (ex. Capping layer). A 75nm thick nitride layer with 1800MPa intrinsic tensile stress on top of S/D is used to study the channel length (L) dependence of the S/D stress component. The resulting average channel stress is captured through the following semi-empirical model (Fig. 2)

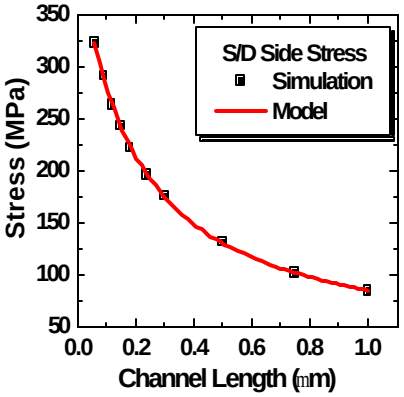

Figure 2: Model fitting to simulated average channel stress transferred from S/D side.

$$S_{AVG}(L) = A1 + \frac{A2}{A3 + L} \tag{2}$$

where *A1*, *A2* and *A3* are the fitting parameters.

Gate-stack side stress can be caused by a stressed gate electrode or stressed gate dielectric or a stressed layer on top of gate electrode. A stressed gate electrode layer (SL) with intrinsic tensile stress of 1800MPa is used to analyze the gate-stack side stress transfer. The *L* dependence of gate-stack side stress transfer is captured through (Fig. 3)

$$S_{AVG}(L) = B1 + \frac{B2}{B3 + L} - \frac{B4}{B5 + L} \tag{3}$$

Process simulations showed that the stress transfer from spacer side is small and hence this component is neglected. In a similar vein, the source/drain length (L_{SD}) can be varied and the model for S_{AVG} as a function of L_{SD} is

$$S_{AVG}(L_{SD}) = C1 - \frac{C2}{C3 + L_{SD}} \tag{4}$$

Combining Eq. 1-4, the stress-induced mobility enhancement model can be expressed as

$$m = m_0 \bullet \left(1 + A1 + \frac{A2}{A3 + L} - \frac{A4}{A5 + L}\right) \bullet \left(1 + B1 + \frac{B2}{B3 + L_{SD}}\right) \tag{5}$$

where μ_0 is mobility model with no stress, *A1-A5* model the *L* dependence and *B1-B3* control the L_{SD} dependence.

Capping layer process is the best test case since it has stress transfer from all three directions. Reduction in hole mobility as a function of channel length is reported in [2] for a tensile capping layer process. BSIM4 model is first fit

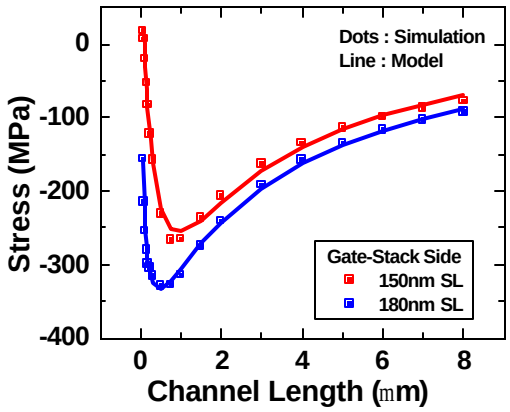

Figure 3: Model fitting to simulated average channel stress transferred from gate-stack side.

to the control wafer mobility. The holistic stress model is then added to reproduce the mobility with the capping layer. Fig. 4 shows excellent fit of the complete model to the experimental data. Fig. 5 shows additional verification of L_{SD} dependence in the model against experimental data for both SiGe S/D and STI process.

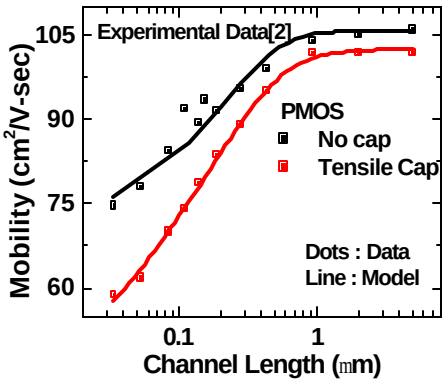

Figure 4: Experimental verification of the holistic mobility model for a capping layer process.

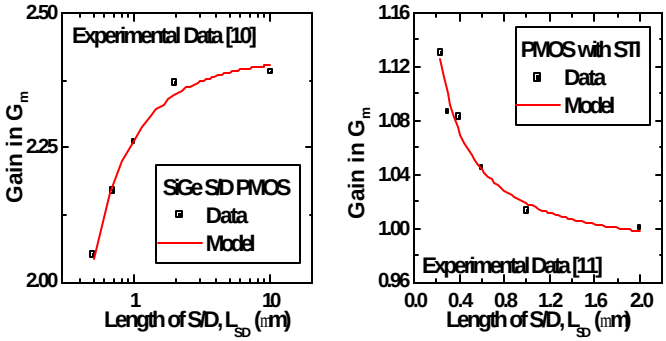

Figure 5: Experimental verification of the holistic mobility model for source/drain length dependence.

3 DYNAMIC BEHAVIOR MODEL FOR HIGH-K MOSFET

High-k transistors exhibit dynamic behavior such as threshold voltage (V_{th}) instability and hysteresis in drain current [12]-[13] due to charging/discharging of the traps in the high-k gate stack [14]. Change in V_{th} of the device is proportional to filled trap density n_T.

$$\Delta V_{th} \propto n_T(t) \tag{6}$$

Using SRH statistics, the rate of change of filled traps in the high-k dielectric can be expressed as [6]

$$\frac{dn_T}{dt} = c_n n(N_T - (1 + A) \cdot n_T) \text{ where } A = \left(\frac{E_T - E_F}{kT}\right) \tag{7}$$

where N_T is the total density of traps, c_n is electron capture constant and n is the electron density in the inversion layer. For the rate equation (Eq. 7) to work under a generalized situation with several traps at different energy levels and different spatial locations, introduce fitting parameters *A1*, *A2*, *C1*, *C2*, *C3* and *C4* as shown below

$$A = A1 \cdot V_g + A2 \cdot V_g^{\,2} \tag{8}$$

$$c_n n = C1 \cdot (1 + C2 \cdot V_{ox}) \cdot \exp\left(-t_{oxe}\left(1 - C3 \cdot V_{ox} - C4 \cdot V_{ox}^{\,2}\right)\right) \tag{9}$$

As V_{th} changes with time, c_n and n vary with time and Eq. 7 is a highly nonlinear differential equation. The rate equation is implemented as a sub-circuit (Fig. 6) in BSIM4 framework with the addition of two nodes. Fig. 7 shows that the model can fit experimentally measured V_{th} shifts.

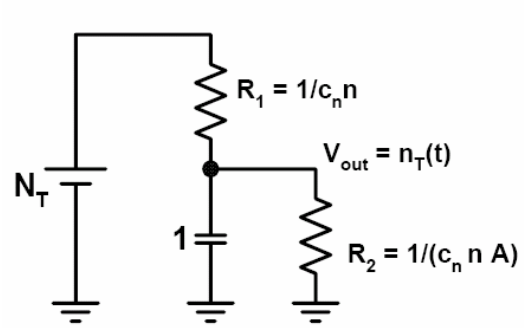

Figure 6: Sub-circuit to implement the nonlinear differential equation Eq. 7 in BSIM 4 framework.

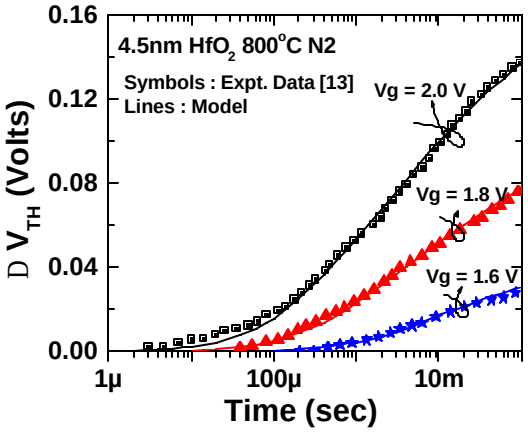

Figure 7: Verification of the dynamic behavior model for the high-k transistors.

4 MULTI-GATE MODEL

An analytical model based on charge sheet approximation has been developed for the planar symmetric DG-FET with finite body doping. The 1-D Poisson's equation including both inversion carriers and bulk charge in the body can be written as

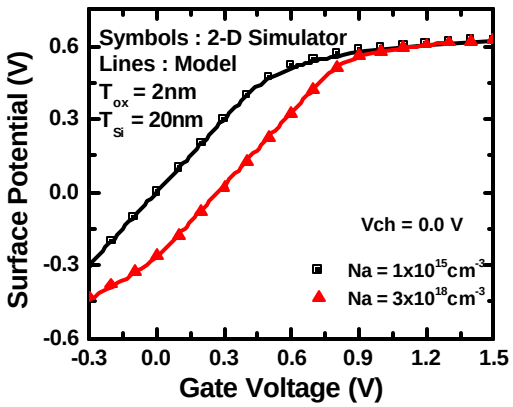

Figure 8: Surface potential referenced to 2-D simulator TAURUS for case of zero channel potential.

$$\frac{d^2 y_s}{dx^2} = \frac{q}{e_{Si}}\left(\frac{n_i^2}{N_A}\exp\left(\frac{q(y_s - V_{ch})}{kT}\right) + N_A\right) \tag{10}$$

where ψ_s is the electronic potential in the body, V_{ch} is the channel potential and N_A is the body doping. Using Gauss's law at surface and the fact that vertical E-field is zero at mid-plane, the Poisson's equation can be solved to yield the surface potential of the DG-MOSFET [8]. Fig. 8 shows that the surface potential calculation from the model agrees well with the simulated value for DG-MOSFET with finite body doping. Volume inversion in the body is captured through the solution of Poisson's equation. Drain current is then formulated using charge-sheet approximation and assuming a fully-depleted body,

$$I_d = 2\frac{mC_{ox}W}{L}\cdot\left(V_g - V_{fb} - \frac{y_s + y_d}{2} - \frac{qN_A T_{Si}}{2C_{ox}} + \frac{kT}{q}\right)\cdot(y_d - y_s) \tag{11}$$

where ψ_s and ψ_d are surface potentials at source and drain, T_{Si} is the body thickness and other symbols have their usual definition. The model can predict the drain current very accurately for DG-MOSFET with finite body doping as shown in Fig. 9.

FinFET can also be fabricated as a triple-gate structure for even better electrostatic control. The model developed for the planar DG-MOSFET is not adequate for the tri-gate structure. The sub-threshold swing and threshold behavior are different in the triple-gate device at the top corners. According to 3-D device simulations, the corner conduction (at top portion) may dominate the sub-threshold leakage current if the channel doping is high (Fig. 10). In addition, the effective vertical field at the corner will be influenced by the two gates. This will cause the mobility near the corner to differ from the mobility of the channel portion that is away fromthe corners.

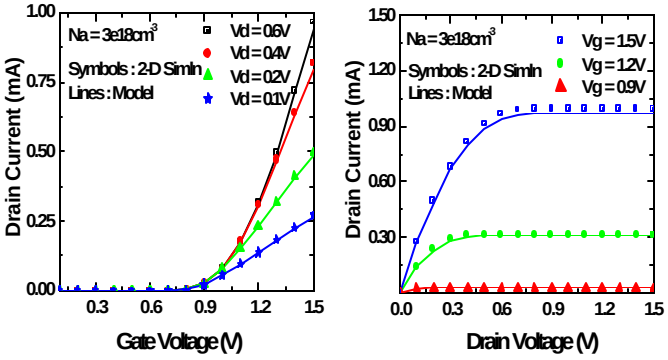

Figure 9: Drain Current characteristics for DG-MOSFET with a finite body doping.

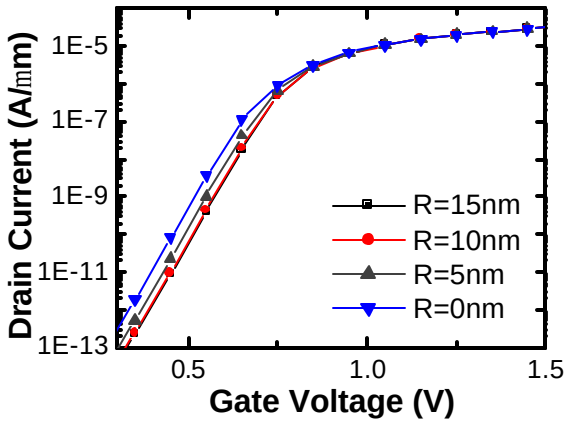

Figure 10: 3-D device simulation of long channel tri-gate transistors with different radius. L_G is 1µm, T_{ox} 1nm, fin height 30nm, fin width 30nm, and N_A 5e18cm^{-3}.

To address these corner effects in the tri-gate structure, modifications to the planar DG-MOSFET model are being investigated.

5 CONCLUSION

BSIM models continue to address the modeling challenges being presented by the new technologies. Mobility enhancement due to process-induced stress in bulk MOSFETs has been modeled for bulk MOSFETs. The model is non-process specific and can handle channel length and source-drain length dependence. A new model to capture the dynamic behavior in high-k transistors has also been developed which can be implemented in BSIM4 framework through a sub-circuit. Finally, a new analytical model for symmetric DG-MOSFET with finite body doping has been developed. The model is being extended to tri-gate structures by capturing the corner effects involved in the device operation.

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