Reproducibility of Silicon Single Electron Quantum Dot Transistor

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ABSTRACT

In principle, based on the form of tunnel junction, single electron transistor (SET) can be classified into four types, i.e. nanowire SET, quantum dot SET, nanotube SET and point contact SET. Another classification is SET based on the kind of conducting material between gate and island, which consists of resistive-SET and capacitive SET. There are about 18 types of SET designs have previously published by many researchers. This paper describes each SET design of 18 all in the reproducibly design point of view at most the form of source-drain contact junction, layers structure, and the modification of fabrication technology. The reproducibility of single electron transistor can be observed from the equity of design, dimension and device characteristics. Indeed, the forms of SET source-drain contact junction have very large influences on the difficulties level of fabrication processes and electrical characteristics.

Keywords: reproducibility, single electron transistor, quantum dot, design of SET, coulomb blockade oscillation.

1 INTRODUCTION

Development of design and fabrication technology of single electron transistor is going on very fast. There are already many designs and fabrication technologies of single electron transistor previously published where each those designs of SETs has strength and weakness. The recent problem in fabrication of single electron transistor is reproducibility of design, fabrication technology and electrical characteristics. There are many factors can affect reproducibility of single electron transistor such as dimension and fabrication technology. Those factors are very important to be considered before we design and fabricate it. Therefore, the knowledge about these factors is needed. We will be benefited from this review of reproducibility of single electron transistor because we can understand varieties of designs of single electron. By reviewing of many single electron transistor designs, we are currently getting information what fabrication methods which applied.

2 DISCUSSION

2.1 Fabrication Technology

A single electron transistor is always three-terminal single electron device (SED), with gate, source, and drain, unlike quantum dots (QDs) and resonant tunnelling device (RTD) which may be two terminal devices without gates [2]. This device is basically composed of 2 electrodes connected to a central Si dot through tunnel oxide junctions. Although the combination of Si technology and the novel structure makes further miniaturization of the Si island possible, reproducible fabrication technology and controllable device characteristics are still being sought by many researchers for realistic application [6]. We feel that it worth considering the reproducible structure of Si based SETs whose electron transport is controlled by a geometrically well-defined Si island in order to optimize their device characteristics (i.e. of voltage gain, operation voltage, switching speed, and integration density) and to estimate the usefulness of their future room temperature counterparts [6]. The process is compatible with SOI MOSFET technology, and offers a way to a reproducible fabrication of Si SET with industrial tools [9].

Remarkably, even in devices for use at cryogenic temperature lower than 4K, in which the requirement for precision in device size can be relaxed, no work has ever shown such reproducibility. It is important to develop a standard way of fabricating devices reproducibly and find out the scaling rule, as is always sought in Si device technology [1].

Silicon thermal oxidation is a stable, reproducible, and controllable process, and therefore PADOX (pattern dependent oxidation) is advantageous for the fabrication of SETs [11]. One of the remarkable features of PADOX (including V-PADOX) is that it offers high controllability of the size of the island and electrical parameters of SETs. For example, gate capacitance can be controlled by changing the structural parameters of pre-oxidation Si patterns [13].

D. Berman et al. (1997) has used modification method between double-angle evaporation and electron beam lithography for fabricating SET and resulted in excellent reliability and reproducibility [5]. Y. Ono et al. (2002) introduced technique for making single-electron transistors,

which uses special phenomena that occur during the oxidation of SOIs, and show that the technique enables them to realize primary single-electron circuits as a result of its high controllability, reproducibility and thermal stability [12]. Y. Ono et al. (2001) point out that control of the oxidation of Si is quite important and could be the key to their fabrication [13].

2.2 Dimension and Design of Single Electron Transistor

The nanowires can be compared to the channel of a field effect transistor. However, as their dimension-thickness and width-are very small the reproducibility of their electrical properties and their FET behavior is not trivial [4]. In spite of efforts to fabricate silicon SET transistors, no work has achieved sufficient controllability in device parameters [1]. However there is a great need for such devices to demonstrate cost-effective processing with high reproducibility, which is typically strongly dependent on feature size. At nanoscales, the control of dimensions by lithography is difficult and hampered by slow throughput [3]. Since control of film thickness is much finer than lateral resolution of lithography, vertical structures can allow precise control of tunnel barrier thickness, which is a critical parameter for current level reproducibility [3].

The planar electrodes have a tip-shape in order to facilitate lift-off. Tip separations ranging from 100 nm down to 20 nm are reproducibly obtained using a thermal-field emission electron source with 5 keV energy and 5 nm point-size e-beam and brushing method [7].

We believe that the excellent controllability in these devices increases the potential of Si-based SET devices for wider range of application because the device parameters are designable, reproducible, and tunable [1].

The main advantage of bilayer is the reproducibility and the high sample yield [8]. We think that the spread in resistance is not due to differences in the bilayer but rather the irreproducibility of the conditions in the vacuum chamber during evaporation [8]. The system also shows excellent stability against changes in external parameters such as humidity and ageing, which is good for the long-term reproducibility of these results [8].

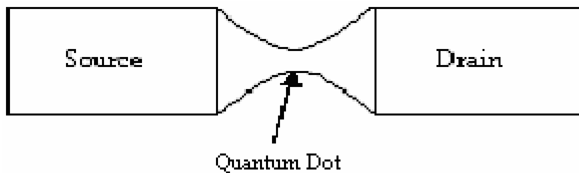

Figure 1. Source-drain contact of quantum dot SET.

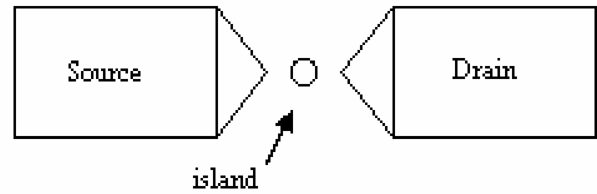

Figure 2. Source-drain contact of lense/dome quantum dot SET.

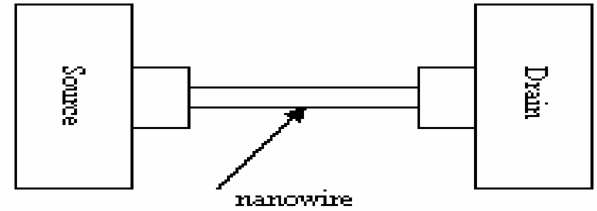

Figure 3. Source-drain contact of nanowire SET.

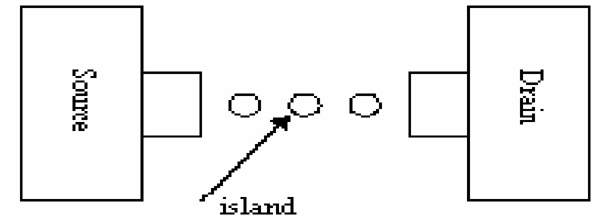

Figure 4. Source-drain contact of lense/dome quantum dot SET.

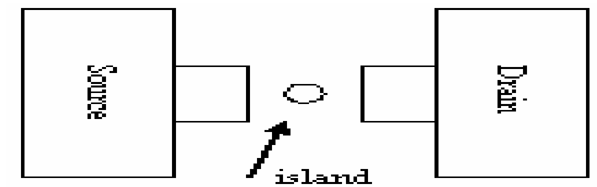

Figure 5. Source-drain contact of lense/dome quantum dot SET.

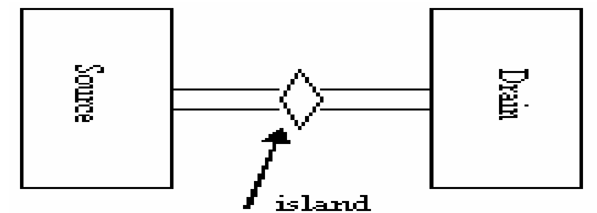

Figure 6. Source-drain contact of square pyramid quantum dot SET.

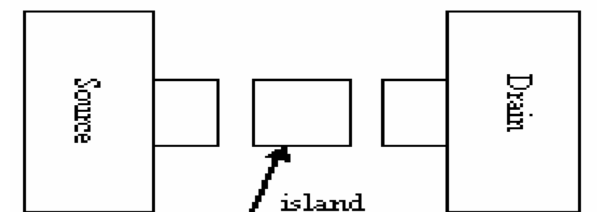

Figure 7. Source-drain contact of truncated pyramid

quantum dot SET.

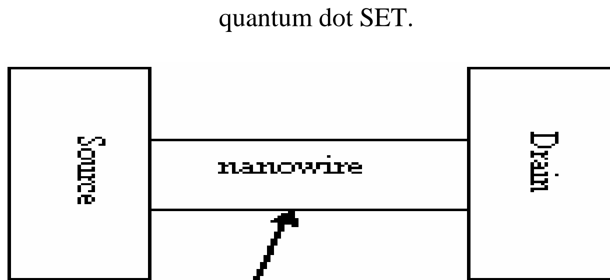

Figure 8. Source-drain contact of nanowire SET.

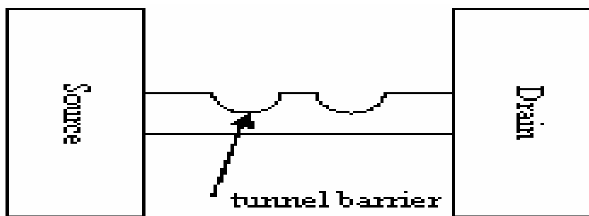

Figure 9. Source-drain contact of nanowire SET with two tunnel barriers.

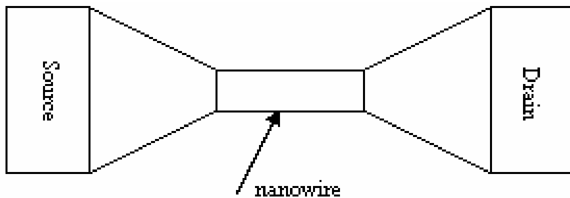

Figure 10. Source-drain contact of nanowire SET.

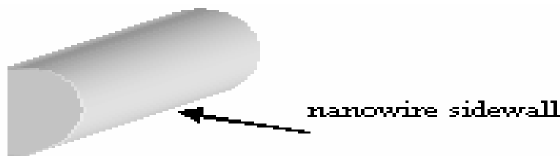

Figure 11. Design of nanowire of SET produced by side wall method.

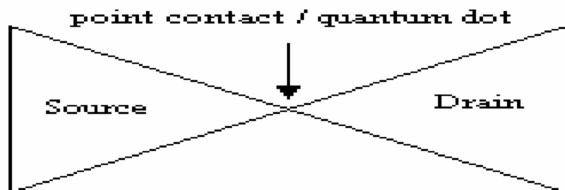

Figure 12. Source-drain contact of point contact/quantum dot SET.

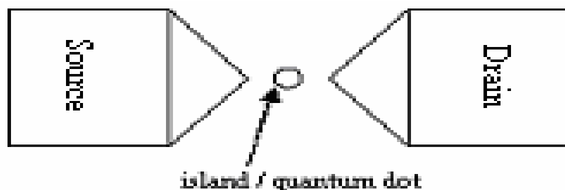

Figure 13. Source-drain contact of quantum dot SET.

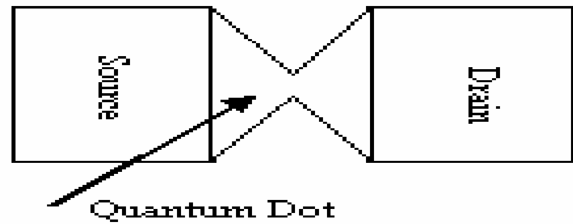

Figure 14. Source-drain contact of quantum dot SET.

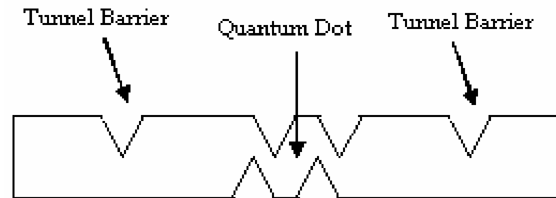

Figure 15. Source-drain contact of quantum dot SET with two tunnel barriers.

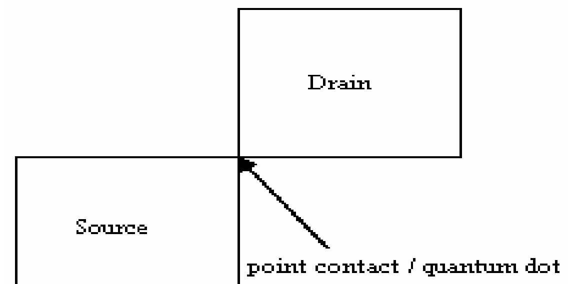

Figure 16. Source-drain contact of quantum dot SET.

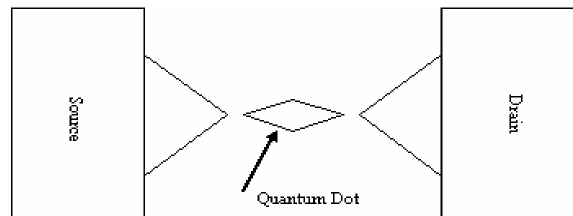

Figure 17. Source-drain contact of elongated pyramid quantum dot SET.

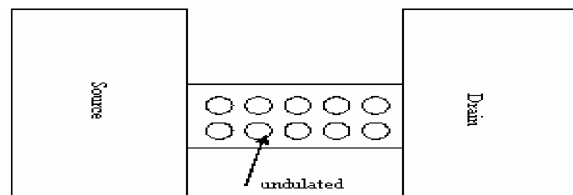

Figure 18. Source-drain contact of undulated nanowire SET.

2.3 Characteristics of Coulomb Blockade Oscillation (CBO)

Akira Fujiwara et al. (2005) obtained excellent reproducibility in the gate capacitances: values on the order of 10 aF, with the variation smaller than 1 aF. This

flexibility and controllability both demonstrates that the device is highly designable to build a variety of SET devices based on CMOS technology [1].

At room temperature the nanostructures have reproducible electrical properties and the fluctuations of the number of the doping atoms do not affect these properties. The use of SOI ensures high quality interfaces and reproducible electrical properties of the structures [4]. The monocrystallinity and the high quality interfaces of the SOI substrates lead to the fabrication of nanostructures with reproducible electrical properties [4].

The fabrication of a reproducible and SOI MOSFET technology compatible silicon SET have been presented. This SET is not small enough to exhibit room temperature Coulomb blockade effects. Nevertheless the combination of width reduction of resist with device oxidation after dot patterning offers perspective for room temperature operating [9].

3 CONCLUSION

We can conclude that high reproducibility of single electron transistor can be achieved by means taking account the following factors: requirement for precision in device size and standard way of fabricating device.

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