

Biocompatible Hybrid System Integration of Silicon Based Neural Interface Devices

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ABSTRACT

Chronically implantable wireless neural interface devices require biocompatible and stable high density integration of several components such as sensing elements, data processors, communication, and power supply coils. Biocompatible integration technology has been developed for Utah Electrode Array (UEA) based implantable neural interface devices. These interface devices comprise: silicon based UEA as sensing element; data processing integrated circuit; surface mounted devices (SMD); inductive power supply and communication coil made of Au and polyimide. Biocompatible materials are used in the flipchip bonding of the components to form a stacked hybrid assembly. In the final step of the device fabrication, the assembled device is coated with SiC and ParyleneC to provide insulating, hermetic, and biocompatible encapsulation. The encapsulation is etched on the sensing tips of the electrodes.

Keywords: UEA, biocompatibility, device-integration, implantable devices.

1 INTRODUCTION

Lately, efforts have been devoted to develop a fully integrated, wireless neural recording device based on the conventional Utah Electrode Array [1,2]. This will free the patients from the risk of infection associated with a wired connection and allow distribution of a network of interface nodes through the central and peripheral nervous system. To this end, fully integrated neural interfaces, Figure 1, need to be biocompatible for chronic (at least one month) implantation. This paper presents the biocompatible materials used in the fabrication and integration of these devices and also the results of the experiments conducted to verify the encapsulation properties of various materials.

2 BACKGROUND

The multi level assembly process uses the 7.8×7.8 mm UEA as the base plate. The backside of the UEA has the under-bump-metallization (UBM) and rerouting

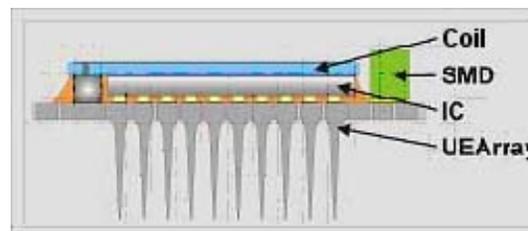


Figure 1: Schematic of neural interface assembly

metallization (RM) layers, Figure 2, to accommodate the IC and SMD components. The UBM consists of sputtered thin film sequence of Pt/TiW/Pt/Au with respective thicknesses of 240/150/250/200 nm. This metallization is to facilitate one-to-one electrical connections from individual isolated UEA electrodes to the signal amplifiers in the IC [3,4], Figure 3. The RM is to bond the SMD components and the power coil. Besides the metal scheme used in the UBM, RM has an additional 100 nm TiW film on the top that serves as a wet-stop on the leads. RM is deposited on the SiN_x passivation layer. The coil for inductive power supply and communication is fabricated by electroplating gold on the polyimide substrate, Figure 4. The coils are glued to the low temperature co-fired ceramic (LTCC) ferrite platelet to increase the Q factor.

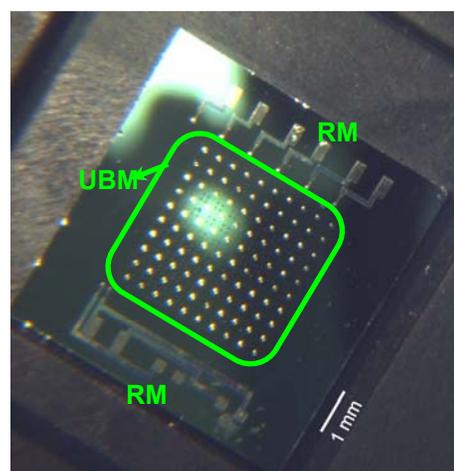


Figure 2: Metallization on the backside of the UEA

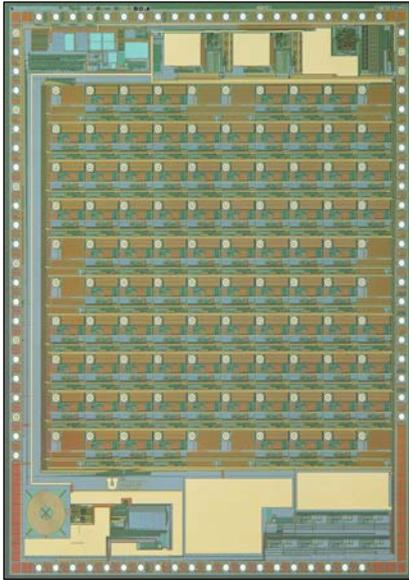


Figure 3: Signal processing chip to be mounted on the UEA

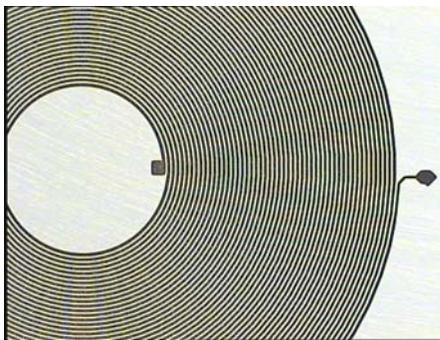


Figure 4: Electroplated Au on polyimide coil for the inductive

3 METHOD

This section describes (a) the integration techniques employed to assemble the neural interface device, (b) experiments conducted to verify the encapsulation properties of the materials used in the integration.

3.1 Integration

To mount the IC on the UEA, Au/Sn reflow flip chip bonding technique is used. As an initial step in this process, nontoxic Au/Sn is electroplated on the IC bond pads to form Au/Sn bumps. Then, force of 10 N at 340°C is applied to reflow the bumps and achieve welding between Au bumps and UBM pads on the UEA. Cu₆Sn₅ alloy solder paste, which has a highly reduced activity, is dispensed on the RM to bond the SMD components. Namics U8433 was selected as underfill material because of its good flow properties even in confined spaces. This material has a

high filler content of 65% silica. Alternatively, a 100 μm thick Au/Sn solder ring can be deposited and sealed during the initial flip-chip bond for the mechanical and chemical protection of the interconnects.

3.2 Compatibility Tests

The compatibility of Namics U8433 to SiC coating was tested. Thermogravimetical measurements showed only a low weight loss of 0.15 % after 2 hours at 200 °C. The adhesion and encapsulation properties of SiC film over the underfill material on a Si wafer were evaluated by storing such a wafer under pressure cooker conditions, ie. 120°C, 100% relative humidity, and 2 bar pressure. The coated wafers have been analyzed in initial state, and as an accelerated test scenario, after by acoustic microscopy. No delaminations/changes could be detected until 72 hours, neither visually nor acoustomicroscopically. After 172 hours cracks in the SiC-layer have been found and investigated using FIB / HiRes SEM. Though SiC is damaged, the bulk underfill layer seems to be intact, Figure 5. It is assumed that a storage duration of 72 hours at pressure cooker conditions without detectable failure is highly promising for the application intended.

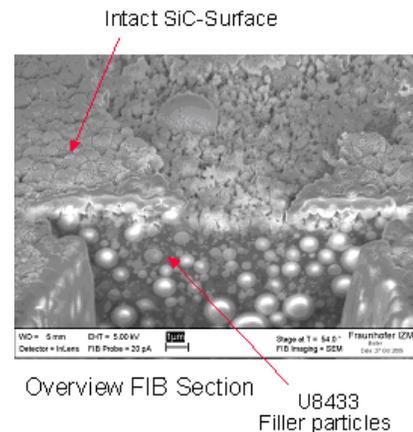


Figure 5: SEM image of FIB section through underfiller and SiC layer

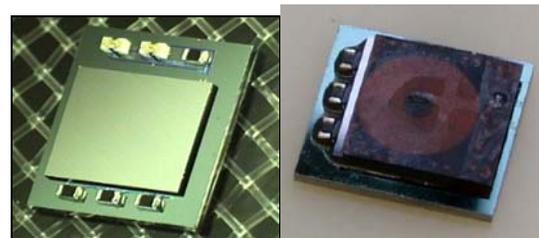


Figure 6: Au/Sn reflow soldered test IC on a test UEA.

3.3 Encapsulation

The hybrid assembly, Figure 6, is encapsulated with hermetic, biocompatible, and insulating SiC and parylene films. Amorphous silicon carbide (a-SiC) was chosen as an innermost hermetic protection layer for the integrated electronics. As additional passivation layer, we are using Parylene C, which has been successfully implemented in many biomedical applications and implants.

In order to investigate the encapsulation behavior and quality of the selected materials (SiC and Parylene C) prior to applying the encapsulation layers on the complete device, silicon based interdigital electrode test structures were fabricated and used for testing, which mimics the geometry and materials of the UEA. Accelerated aging tests (pressure cooker and heated saline solution) were performed to determine and analyze potential failure modes for the layers. Leakage current tests, impedance spectroscopy, dissolution and adhesion tests were performed on both SiC and parylene coatings. The adhesion between SiC and parylene, and sterilization of the encapsulated test structure were investigated.

3.4 Impedance Spectroscopy and Leakage Current Tests

Test IDE structures were prepared and immersed in 0.9% NaCl saline solution. The bottles were maintained at 37°C. After five days the structures were investigated using impedance spectroscopy (50 mV AC, Solartron 1255 Frequency Response Analyzer, Solartron 1287 Electrochemical Interface).

Plasma-enhance chemical vapor deposition (PECVD) grown a-SiC:H and CVD grown Parylene thin films were deposited on oxidized silicon and quartz substrates with a Ti/Pt (50 nm/330 nm) interdigital electrode (IDE) structure. The electrical properties of the encapsulation materials were measured by impedance spectroscopy. These test structures were placed into Ringer's solution at 37 °C for aging test over a period of 3 to 4 months. Material degradation, adhesion failure, electrical short circuits in the interface between encapsulation and substrate and bulk encapsulation material property changes will lead to impedance/capacitance change during the test. It was shown that the impedance remain unchanged up to 3 months for SiC (Figure 7) and 4 months for parylene coated IDEs (Figure 8). The tests were discontinued because the copper leads corroded and disconnected from the IDE chip. A better test set up was built for longer encapsulation properties evaluation.

Leakage current tests were performed for 1 month on each sample using a voltage of 5V DC. The investigation of leakage currents on the SiC and Parylene C layer combination showed a current of about 10^{-12} A to 10^{-11} A at the beginning of the filled sample bottle (0.9% NaCl). The first three days were measured without physiological solution as a control test. After one month, the current still

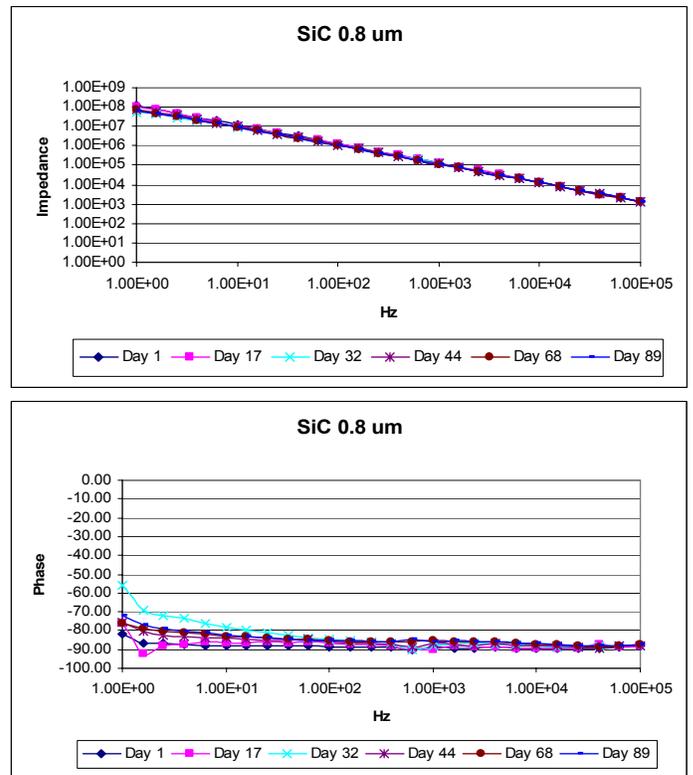


Figure 7: Long-term impedance spectroscopy of 0.8 μm SiC coating in Ringer's solution at 37 °C

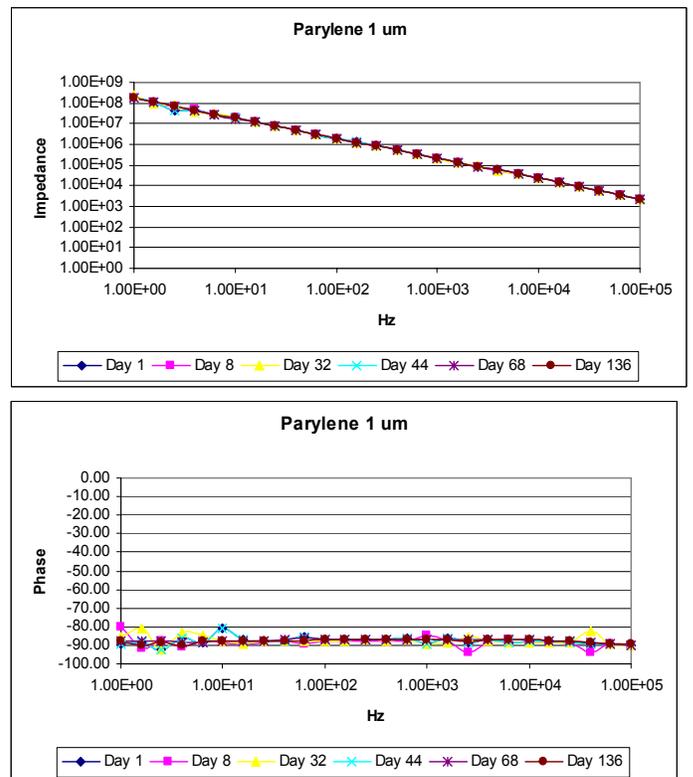


Figure 8: Long-term impedance spectroscopy of 1 μm parylene coating in Ringer's solution at 37 °C

remained in the range indicating no corrosion or delamination of the IDE structure, Figure 9.

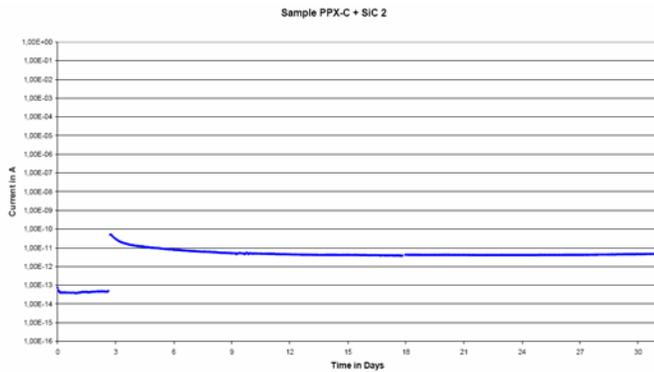


Figure 9: Leakage current measurement of still functional encapsulation sample (PPX-C and SiC combination).

4 CONCLUSION

A reliable hybrid integration technique has been developed for the implantable microdevices. The process makes use of the biocompatible combination of materials, takes into account process compatibility, electrochemical effects and stability in electrolytic environments and may serve as a general technology base for high density interconnects for implantable microdevices. Encapsulation properties of SiC and ParyleneC have been tested by impedance spectroscopy and leakage current electrical measurements. Adhesion and dissolution tests were conducted to evaluate film degradation, delamination, and dissolution respectively. Results indicate that these materials can provide adequate biocompatible encapsulation to implantable microdevices.

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