A Nano-Scale Module with Full Spin-Wave Interconnectivity for Integrated Circuits

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ABSTRACT

In this paper, we present a nano-scale spin-wave-based fully interconnected architecture, in which each node can simultaneously broadcast to all other nodes, and can concurrently receive and process multiple data. This design allows nodes to intercommunicate in constant time, and has an $O(N^2)$ area. Here, unlike traditional spin-based architectures that transmit charge, the information is encoded into the phase of spin waves. As a result of this, the presented nano-scale design may have low power consumption.

Keywords: nano-scale architectures, fully interconnected networks, spin waves.

1 INTRODUCTION

During the past several decades, many multi-processor VLSI chips have been proposed with the goal of obtaining optimal speed-ups in minimal area. Nevertheless, the desired speed-ups are not always realizable due to certain inherent limits in the VLSI technology. For example, the VLSI area of a fully interconnected network of multiprocessors on a chip, in which each of the computing nodes can send (or receive) data to (or from) all the other nodes directly and in constant time, is in the order of $O(N^4)$, which would be unreasonably large to implement. Furthermore, the implementation of such an organization will require having nodes with O(N) fan-in fan-out, which also is not practical in VLSI. If constant degree nodes were to be used instead, then there would be an $\Omega(\log N)$ intercommunication delay lower-bound in realizing such a network in VLSI using electrical interconnects. The replacement of electrical wires with free-space optical interconnects, though, can significantly improve the VLSI area and fan-in fan-out limitations [1]. However, electro-optical designs have their own challenges, especially with respect to switching issues [2].

Another alternative for reducing the VLSI area requirement is to use nano-scale architectures. Several methods have been proposed during the past few years for the design of such chips. Among them are designs having single electron transistors, molecular switches, quantum-dots, carbon nano-tubes, and spins [3]. In traditional spin-based devices, information is stored into spins as a spin orientation (along with or opposite to the external magnetic field). The spins, attached to carriers, transfer information from one spin-based device to another through a conducting wire. We propose to use spin-wave-based devices in which the wave transmits the information without any charge transfer.

The architecture presented here is a nano-scale fully interconnected one in which each node can broadcast using spin waves to all other nodes simultaneously and, similarly, each node via spin waves can receive and process multiple data in parallel. The significance of this design is that the communication between the nodes can be done in constant time, which is a significant improvement considering the $\Omega(\log N)$ lower-bound on the time delay for implementing such networks in VLSI using traditional electrical interconnects. Moreover, this fully interconnected network can be laid out in $O(N^2)$ area as opposed to $O(N^4)$, and of course the unit of area is in order of nanometer as opposed to the standard micron technology that is currently in use. In this architecture, information is encoded into the phase of spin waves, and charge is not transmitted. As a result of this, power consumption may be significantly reduced in this architecture as opposed to other nano-scale architectures.

The rest of the paper is organized as follows: In section 2, we present a brief introduction to spin-waves. We then describe our proposed spin-wave-based fully interconnected architecture in section 3, which is followed by our conclusion and future work in section 4.

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2 PRELIMINARIES ON SPIN WAVES

Spin waves have been attracting scientific interest for a long time, but only recently were there several experimental types of projects devoted to the problem of spin-wave detection using the inductive voltage measurement technique [4,5]. The results indicate that spin-wave packets propagating in a 100-nanometer-thick ferromagnetic film may produce an inductive voltage in the order of several mV, suitable for experimental detection [5]. The inductive voltage measurement technique appears to be one of the most convenient physical methods for spin-wave detection and integration in a semiconductor platform.

The use of spin waves for computation is an entirely new idea. The first computational architecture utilizing spin waves for massive entanglement of distant spin-based qubits in a quantum computer was described in earlier publications [6,7]. Later in another publication [8], and here, too, spin-waves are used for both information transmission and information processing. We employ the classical type of computing as opposed to quantum, and the architecture presented can operate at room temperature.

In the ideal case, spin waves can be used to provide an "LC" coupling of devices, without dissipative resistance. With the spin-wave concept, the spin rotates as a propagating wave and there is no particle (electron/hole) transport [8]. In Figure 1, we have schematically shown the prototype of the spin-wave-based logic device structure being built at our nano lab in UCLA. The core of the structure consists of a 100nm-thick CoFe film deposited on a silicon substrate. There are two asymmetric coplanar strip (ACPS) transmission lines on the top of the structure. The distance between the lines is 8μm. The lines and the ferromagnetic layer are isolated by 300nm silicon oxide layer. The dimensions of the ACPS lines are adjusted to match 50Ω of the external coaxial cable. One of the ACPS lines (shown on the right) is used for spin-wave excitation. Hereafter, we will refer to this ACPS line as the "excitation" line. A voltage pulse applied to the excitation line produces a magnetic field and excites a spin-wave (spin-wave packet) in the ferromagnetic layer. Being excited, spin-wave propagates through the ferromagnetic film. The other ACPS line (shown on the left) is used to detect the inductive voltage signal produced by the propagating spin-wave. Hereafter, we will refer to this line as the "detection" line.

In Figure 2, we present the experimental data on spin-wave detection by the time-resolved inductive voltage measurement technique [9]. The dashed line depicts the voltage pulse applied to the excitation line. The pulse characteristics are as follows: pulse amplitude 24.5V; rising time 1.2ns; and pulse length 20ns. The solid line depicts the inductive voltage signal detected by the detection line. One can see the inductive voltage oscillation at the detection line caused by the inductive coupling via the spin waves. The output voltage signal has maximum pulse amplitude 26mV, and the period of oscillation is 9ns.

These experimental data illustrate the possibility of signal transmission by spin waves over micrometer range distances. The attenuation time is about 20ns, and the signal-to-noise ratio is satisfactory (at least for 8μm propagation distance). We would like to stress that the utilization of spin waves is prominent for short-range in-chip communication. There are several important issues that require additional consideration: (i) power dissipation in the spin-wave bus, and (ii) signal gain. In principle, the energy per spin wave can be scaled down to several kT, to be just above the thermal noise level. On the other hand, in order to compensate for the damping of spin waves, one needs to include an amplification mechanism (gain). One of the possible gain mechanisms may be parametric spin-wave amplification, which has been experimentally demonstrated [10].

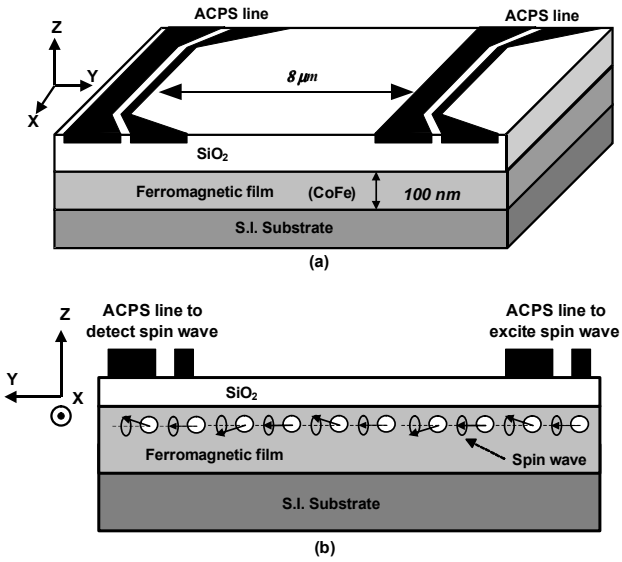

Figure 1- Prototype of the Logic Device Structure

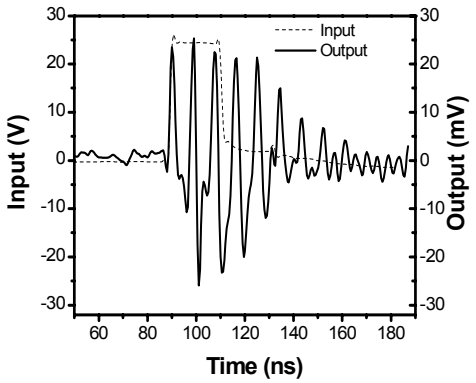

Figure 2- Experimental Data on Spin-Wave Detection

3 THE ARCHITECTURE

In this section, we present an overview of our fully interconnected architecture with spin waves. Figure 3 shows the top view of the architecture in which the N computing nodes are placed around a circle on a magnetic film. Each node is an ACPS line, which can be used as a sender or receiver at each point of time. Figure 4 shows the cross view of the layout of this architecture on a semiconductor chip. The area requirement of this architecture is $O(N^2)$ as opposed to the $O(N^4)$ area requirement if electrical interconnects were to be used. We should also note that all the distances in this architecture are in nano-scale. Also, unlike electrical interconnection networks, in which only one transmission can be done at a time, here multiple simultaneous permutations are possible by transmitting the spin waves over different frequencies. The information is coded into the phase of the spin waves in the sender and is detected by the receivers. In addition, within each frequency, data can be sent to one or more other nodes from each node. In the following, we present a brief discussion about the placement of nodes and the communication mechanisms among them.

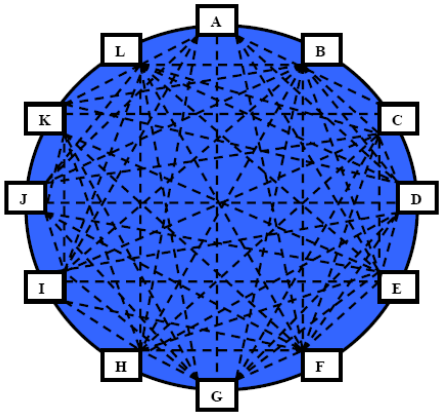

Figure 3. The top view of the architecture with full spin-wave interconnectivity

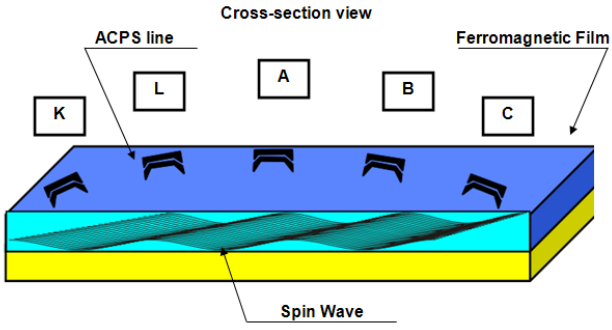

Figure 4 - Cross-section view of the architecture with full spin-wave interconnectivity

3.1 - Placement of the nodes

Normally, in architectures where the phases of the waves are the means of information transmission, the exact location of the nodes with respect to the size of topology is an important design issue. The distance between the sender and receiver has to be at a length that is a multiple of the wave's wavelength; otherwise the receiver might receive the wave with a π radian phase-shift, which is a "0" instead of a "1" or vice versa. However, in our design, this is not an issue because the wavelengths of spin waves are considerably larger than the distance between the nodes. The speed of spin waves is around 10^5m/s. Assuming the input frequency range of 1-10 GHz (as in our experiment), the wavelength will be in the order of 10^{-4} to 10^{-5}m, while the distances are nano-scale or 10^{-9}m. In other words, the wavelengths of the spin waves are some orders of magnitude greater than the distances between the nodes. Therefore, all the nodes receive the same phase regardless of their location, and there is no need to place the nodes in specific distance relative to the other ones.

3.2 - Communication among the nodes

In this architecture, as shown in the top view, each node can broadcast to all other nodes simultaneously. For instance, node A can broadcast to all the other nodes. This requires that all the nodes' receiving frequencies to be tuned on the same frequency as the node A's transmitting frequency. Similarly, a node can receive and process multiple data simultaneously. For instance, node G can receive multiple data simultaneously from other nodes. In this case, the requirement is that all the nodes should transmit at the same frequency that is also the frequency at which G's receiver is tuned.

To distinguish the data being transmitted to different nodes, transmissions are done at distinct frequencies. In a way, this is similar to having various radio stations, each broadcasting at a different frequency. To listen to a specific station, one tunes to the corresponding frequency. Here, similarly, each node can broadcast or receive at a specific frequency. Furthermore, at a given frequency, a node can listen to multiple waves simultaneously. Using the superposition property of waves, it can compute the sum of all waves destined to it.

In addition to the transmissions at different frequencies, all nodes in this architecture can work on the same frequency in a broadcast mode, or they can be directed to specific locations using phased array techniques [11]. It is also possible to combine the phased array technique with multiple frequencies. This way, for each frequency, some of the waves are only transmitted to desirable directions and are received by the intended sources.

3.3 - Data detection at the nodes

In our architecture, the communication is done via spin waves, but the computation is done electronically. When mapping an algorithm to this architecture, one should take into consideration the fact that once the spin waves are detected by the receiver ACPS lines, the transmitted data can either be digitized or they can be left analog.

First, the input information is coded into the polarity of the voltage pulse applied to the edge ASPC lines (for example, V_{input} = +1V corresponds to the logic state 1, and V_{input} = -1V corresponds to the logic state 0). Next, in order to detect the output signal V_{ind} we use the time-resolved inductive voltage measurement.

In analog detection mode, the ACPS line detects the inductive voltage produced by the *superposition* multiple waves. For example, if ten waves are sending a "1," then their analog sum through their cumulative amplitude is computed instantly as 10. Also, this property can be used to compute logical functions as described previously. In digital detection mode, this value is digitized to just a "1," and then the computations are continued digitally.

It is possible to realize different logic gates AND, OR, and NOT controlling the *relative phase* of the spin waves. The voltage measured in the output port is compared to a reference voltage to determine logic state 1 or 0. This measurement is performed at the moment of spin-wave packet arrival to the detecting ACPS line area. For more information, refer to related publications [8,12].

4 CONCLUSION

In this paper, we presented a nano-scale spin-wave-based fully interconnected network, in which each node can broadcast to all other nodes simultaneously and, similarly, each node can receive and process multiple data at the same time. The significance of this design is that the communication between the nodes can be done in constant time, which is a significant improvement to the $\Omega(\log N)$ lower-bound on the time delay that existed for implementing a similar structure with electrical interconnects and bounded degree nodes on a VLSI chip. Moreover, using spin-wave-based interconnection, this fully interconnected network can be implemented in $\Theta(N^2)$ "nano-scale" VLSI area, as opposed to $O(N^4)$ for a VLSI chip with electrical interconnections. In our architecture, information is encoded into the phase of spin-waves, so unlike traditional spin-based architectures, charge is not transmitted. This results in another key advantage of our design, the low power consumption. The basic mechanism for operating this type of architecture was described. We also presented our preliminary experimental results towards fabricating such a design. A future application of this architecture would be in designing implantable biomedical devices. More details appear in our related papers [12] and the full journal version of this paper.

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