Synthesis and Electrical Characterization of Silicon Nanoparticles for Electronic Applications

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Single-crystal nanoparticles of silicon may be suitable as building blocks for single-nanoparticle electronic devices. To assess their potential for future nanoelectronic devices, we have fabricated silicon nanoparticle Field Effect Transistors (FETs) using the nanoparticles as the active layer. The goal of this study is to show the semiconducting nature of the nanoparticles and to characterize the performance of nanoparticle FETs. The electrical characteristic measurements of these devices show that changing the voltage applied to the gate can vary the current flowing through the transistor. The source-drain current decreases with increasing gate voltage, which demonstrates that the device operates as p-channel FET. Based on the transfer characteristics obtained for different source-drain voltages, the carrier transport in the nanoparticle devices appears to be diffusive. The devices fabricated show good performance characteristics indicating potential for application in nanoelectronics.

Keywords: silicon nanoparticles, electrical characterization, FETs

Silicon nanoparticles due to their unique properties that display size-dependent quantum effects are widely considered a promising material for a wide range of applications and novel devices. The quantum size effects and the coulombs blockade phenomenon make the nanoparticles extremely attractive to use in functional devices such as single electron transistors [1], vertical transistors [2], resonant tunneling devices [3-4] and floating gate memory devices [5-8]. Nanoparticles have been produced by plasma enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), and laser ablation [9]. However, there is little research in the way of the particle electrical characteristics. In general, this has involved building a composite structure of nanoparticles embedded in an insulating matrix [10] or measuring the electrical properties of freestanding nanoparticles by making two direct electrical contacts using scanning tunneling microscopy [11-12] or atomic force microscopy [3].

Due to the strong carrier confinement in a silicon nanoparticle it is reasonable to assume that the electrical properties of these particles will be different from their thin film equivalents. For example, the current through a nanoparticle can vary by several orders of magnitude when the addition or removal of a single electron changes the charge on a nanoparticle. Since the location of nanoparticles is random, a critical step is nanoparticle device fabrication that allows for the exploration of electrical properties of nanoparticles. In our approach we have used a three-dimensionally confined nanoparticle embedded in a simple bottom gate field effect transistor device. In this paper we review the process to synthesize single-crystal silicon nanoparticles in an LPCVD chamber and characterize the electrical properties of these nanoparticles and examine their carrier transport mechanism.

The silicon nanoparticles used in this study were deposited on SiO_2 substrate by thermal decomposition of silane using Low Pressure Chemical Vapor Deposition (LPCVD) [13-17]. Varying the time, temperature and partial pressure of silane gas can change the average diameter and height of the hemispherical nanoparticles formed. This route offers an excellent control over particle size and size distribution and particle density. The nanoparticles were imaged using Atomic Force Microscopy (AFM) in the tapping mode, Figure 1. The nanoparticle diameter was in the range of 20-30 nm while the height was in the range 15-25 nm. This approach, also allows the fabrication of both n-type as well as p-type devices by doping the nanoparticles during deposition. Nakajima etal. used Transmission Electron Microscopy (TEM) to show that the core of the silicon nanoparticles deposited using the above method is crystalline with a diamond structure [14].

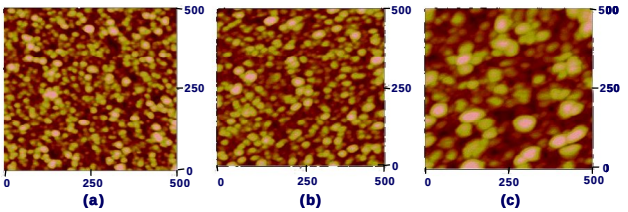

Figure 1: Atomic Force Micrographs (scale - nm) of silicon nanoparticles grown on HF treated silicon dioxide substrate for LPCVD deposition times of (a) 1, (b) 2, and (c) 6 min. The growth parameters are at 625ºC and 0.25 Torr deposition pressure

Field Effect Transistors were fabricated with silicon nanoparticles as the active layer. A schematic cross section of the nanoparticle field effect transistor (N-FET) device is shown in Figure 2. The N-FET consists of layer of nanoparticles bridging two electrodes deposited on a 200 nm thick gate oxide film on a highly doped silicon wafer, which is used as a back gate. The 200 nm thick aluminum electrodes were deposited using conventional photolithography. For electrical characterization, the current-voltage (I-V) and transfer characteristics through the nanoparticles were measured at room temperature as a function of bias voltage V_{SD} and gate voltage V_G.

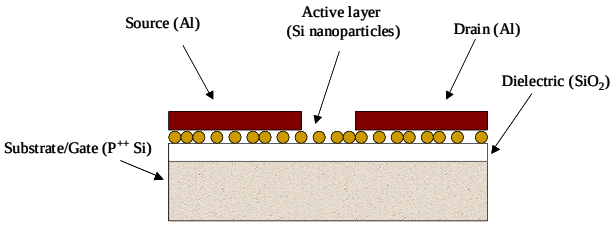

Figure 2: Schematic cross-section of bottom gate device showing the gate and source and drain electrodes.

Electrical measurements were performed on the sample devices using the substrate at the bottom gate. Figure 3 shows the output characteristics for the bottom gate device with a gate oxide of 200 nm. Figure 3(a) shows the IV characteristics of the N-FET device with gate voltage being swept from 2.0 V to –5.0 V. The maximum transconductance is 7.05 nS. The transfer characteristics (Figure 3(b) I-V_G of our N-FET device shows a behavior similar to that of a p-channel metal-oxide-semiconductor FET. The source-drain current decreases strongly with increasing gate voltage, which demonstrates that the nanoparticles device operates as a field effect transistor but also that the charge transport is due to positive carriers. The linearly extrapolated threshold voltage is 0.9 V. However for $V_G<0$, the I-V_G curves do not saturate; instead the drain current (I_D) decreases exponentially with V_G. Because when the gate voltage is below the threshold voltage and the semiconductor surface is only weakly inverted, the drain current is probably dominated by diffusion instead of drift. This is called the subthreshold region [18]. This shows that the N-FET device can be used as a low-voltage, low-power device, such as a switch in digital logic and memory applications.

Having demonstrated FET operation for silicon nanoparticles, we move on to explore whether the electrical properties of the N-FET are affected by the change in nanoparticle density. Figure 4 shows a comparison of the output characteristics for a N-FET device with two different nanoparticles densities and sizes. The lower density of

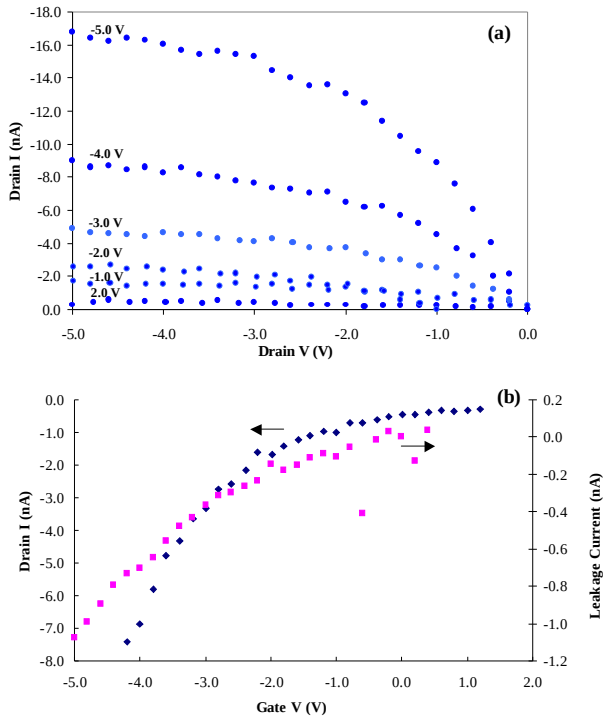

Figure 3: (a) I-V characteristics of bottom gate p-type N-FET with Al gate and gate oxide of 200 nm. The gate voltages range from 2.0 to –5.0 V. (b) Transfer characteristic of N-FET for VDS of –2.0 V and Leakage current for gate voltage from 2.0 to –5.0 V.

nanoparticles also indicates larger size both in height and diameter. Although the N-FET device with high nanoparticle density shows higher drain current for lower gate voltages, at higher gate voltages it appears that the density of the nanoparticles does not affect the performance of the device. This also indicates that fundamentally the conduction properties of the nanoparticles do not depend on the size or density of the particles.

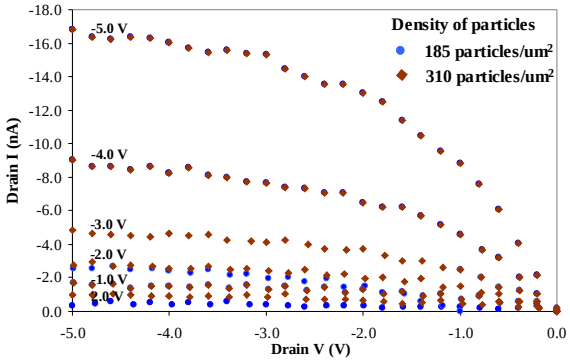

Figure 4: Output characteristics of p-type N-FET with different nanoparticle densities

In conclusion, we have fabricated silicon nanoparticle-based FET that act as p-type semiconductors. These devices can be used in the sub threshold region as low-voltage and low-power devices. Although there are many challenges ahead before N-FETs can be used for real technological applications, our results indicate that nanoparticle based devices are promising in the future.

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