A Novel Approach of Sample Preparation for SCM Inspection in the DRAM Device Structures

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ABSTRACT

This paper discusses the removal of the doped polysilicon of a gate transistor by KOH wet chemical etching containing the spacer oxide and nitride that remain. This technique significantly improves the image quality of a two-dimensional (2-D) doping profile of scanning capacitance microscopy (SCM), which more accurately provides the results of the desired device structures for inline monitoring, failure analysis, and also for product characterization.

Keywords: deep trench, DRAM, SCM, 2-D doping profile, KOH

1 INTRODUCTION

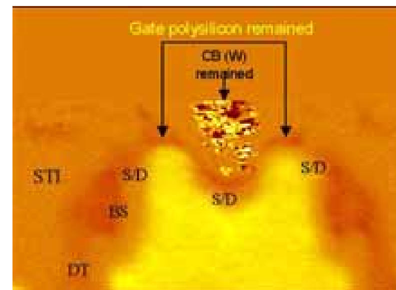
Scanning Capacitance Microscopy (SCM) has been proven for years to be one of the useful analytical tools for two-dimensional (2-D) carrier profiling in semiconductor device structures that are used for failure analysis and characterization [1-2]. However, the sample preparation of a cross-sectional surface for SCM inspection is always a challenge for a failure analyst to obtain a quality 2-D carrier profile.

Using the traditional sample preparation method for the cross-sectional doping profile of SCM (Figure 1a) in the memory array of an advanced deep trench (DT) capacitor DRAM [3], the doped-polysilicon of a gate transistor could interfere with the 2-D doping profile in the source/drain regions during SCM imaging. That disturbs the finding of possible failure causes, the measuring of effective channel lengths (L_{eff}) and junction depths.

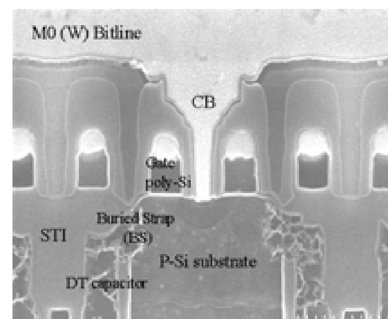
In order to eliminate the interference of the doped ploysilicon with junction profiles, we explored a new method of sample preparation to improve the image quality of a 2-D doping profile of SCM. This more accurately provides the results of the desired device structures for inline monitoring, failure analysis and also for product characterization.

2 EXPERIMENTAL PROCEDURE AND DISCUSSION

The DRAM chip was prepared using a Si (100) wafer for this study. The conventional de-processing method of chemical wet etching and mechanical polishing was applied to the desired chip. After the chip was stripped to a M0 tungsten (W) layer or a gate transistor level, the desired device in an advanced deep trench (DT) capacitor DRAM was localized and marked by the FIB/SEM system. Then the cross-sectional SCM sample of the desired device was made, employing the standard mechanical polishing techniques, finishing with a 0.05 μm colloidal silica emulsion. The sample was heated at around 200 ℃ for 20 minutes in an ambient atmosphere to form a high quality surface oxide layer. It was then illuminated under a high-density ultraviolet (UV) light for 1 minute to remove any trapped charges in the surface oxide.



(a)



(b)

Figure 1: (a) A typical SCM image of an NMOS gate array device created by the conventional procedures of SCM sample preparation. The gate polysilicon remains on the gate oxide of the gate transistor. (b) A cross-sectional SEM image showing the structure of Fig. 1a in a deep trench capacitor DRAM cell.

The SCM images of the 2-D doping profiles of the desired DRAM device structures were obtained using a commercial DI-3100 Atomic Force Microscope (AFM) equipped with an SCM application module. A 0.5V AC bias at 90 KHz and a 0.0V DC bias between the conductive tip and the sample were used for this analysis.

Fig. 1 shows a typical SCM image of a NMOS gate array device created by the conventional procedures of SCM sample preparation and a corresponding cross-sectional SEM (scanning electron microscopy) image of this device. The N-type doped-polysilicon remains on the gate oxide of the gate transistor. The SCM image demonstrates the differently doped areas of the transistor (source, drain and gate), capacitor (DT), connection (BS) of capacitor and transistor, and Si substrate. However, the effective channel length and the junction depth cannot be resolved clearly from this image. This probably was caused by the noise of the doped ploysilicon that interfered with the junction profiles.

In order to improve this SCM image quality, a new approach was developed. After the conventional de-processing procedures (the sample was stripped to the level of a gate polysilicon), this invention removed the doped-polysilicon of a gate transistor at the desired sample surface by the KOH wet chemical etching. The doped-polysilicon of a gate transistor was removed but the spacer oxide and nitride remained as shown in Figure 2. The remaining spacer oxide and nitride could be used as a reference for counting to a specific site and for recognizing the relative position of the S/D to the gate during the SCM imaging.

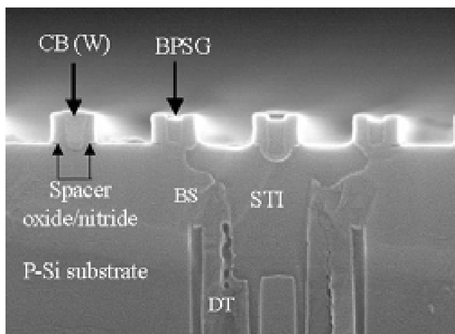


Figure 2: A cross-sectional SEM image showing the structure of a deep trench capacitor DRAM cell after the polysilicon of a gate transistor was removed by KOH. The spacer oxide and nitride remains.

By following the standard mechanical polishing techniques for the cross-sectional SCM sample, the 2-D doping profile at a specific site of the device structure can therefore be revealed more accurately by SCM inspection. Figure 3 shows the typical SCM image created by the new sample preparation method at the same NMOS gate array device as that shown in Fig. 1. The SCM image indicates that the quality of the 2-D doping profile is improved significantly on the differently doped areas compared with that of Figure 1a. The contrast between the N- and P-type doped regions clearly delineates the boundary between them. The effective channel length and the junction depth of this device by this method can therefore be resolved more accurately than that of the conventional method.

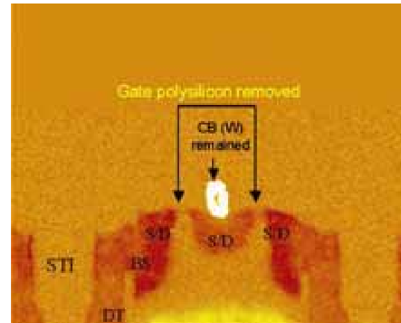
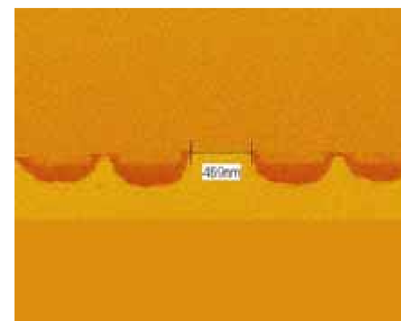
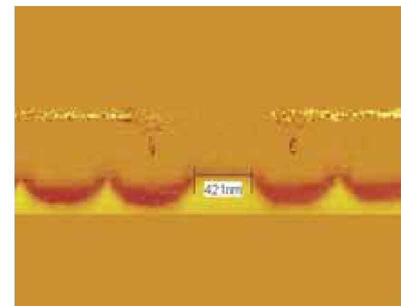


Figure 3: A typical SCM image of an NMOS gate array created by the new method. The gate polysilicon over the gate oxide of the gate transistor is now removed.



(a)

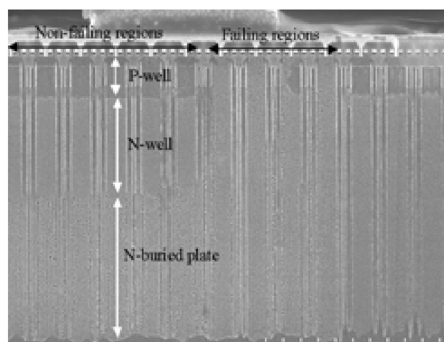


(b)

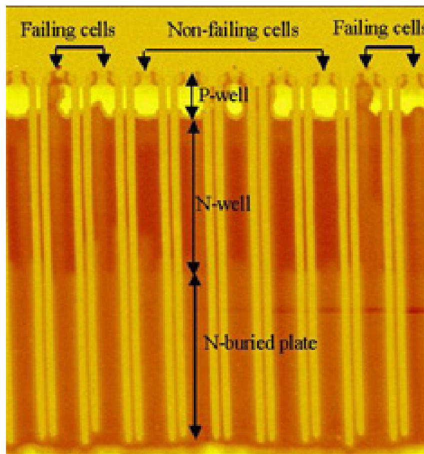
Figure 4: SCM images of a 0.6um gate length n-MOSFET created by (a) the new method and (b) the conventional procedure.

This technique has been applied for the inline monitoring and failure analysis in our laboratory. In one example, the physical L_{eff} was measured for verifying the electrical L_{eff} measurement in the test structures. The

calibration of L_{eff} between electrical measurement and SCM physical measurement in the device was made during the process development. While the electrical measurement of L_{eff} shows an abnormal trend at a particular device, the SCM physical check is required to verify the result. Fig. 4 shows SCM images of a 0.6um gate length n-MOSFET created by the conventional procedure and this new method. The L_{eff} of this device obtained by the new method (Fig. 4a) is measured at 469 nm, which is 11.4 percent more than that (approximately 421 nm) of the conventional method (Fig. 4b). This 11.4 percent error created by the sample preparation now becomes an important factor in justifying the causes and correcting the problem in the process. To produce more accurate and consistent SCM results in a proper way, this new approach is required.



(a)



(b)

Figure 5: (a) The SEM image and (b) the SCM image showing the doping profiles at both the non-failing areas and the failing areas.

In another example, the doping profile was examined for failure analysis. One of the failure modes, called a "cluster SCFs (single cell failure)", was detected during the electrical test. From the inline data review, the failure mode that occurred in this case was correlated to the ASG (arsenic-silica glass) related processes that were used to form a N-buried plate [3]. The SEM image (Figure 5a) shows the differences of contrast between the non-failing areas and the failing areas in the regions of the P-well and N-well. Furthermore, the SCM image (Fig. 5b) indicates the N-type doping species had been out-diffused into the P-well and N-well in the areas of the failing cells during the process. This was caused, in the process, by the ASG residuals that remained above the depth of N-buried plate. In the process flow, the ASG in the trench walls above the depth of the N-buried plate must be stripped away completely before we conduct the process of ASG out-diffusion to form the N-buried plate. As we formed the N-buried plate, the remaining ASG in the trench walls was then out-diffused into the Si substrate of the P-well and N-well regions to cause the failures. The root cause of this failure has been verified from the results of failure analysis and this problem has been corrected in the manufacturing process.

3 SUMMARY

A novel approach has been developed to significantly improve the image quality of a 2-D doping profile of SCM. The removal of the doped polysilicon of a gate transistor by KOH wet chemical etching eliminates the interference of the doped ploysilicon with the junction profiles. The remaining spacer oxide and nitride could play a role as a reference for counting to a specific address and for recognizing the relative position of S/D to the gate. This method more accurately provides the results of the desired device structures for inline monitoring, failure analysis, and also for product characterization.

4 ACKNOWLEDGEMENTS

The authors would like to present our thanks to the colleagues at the Department of Physical Failure Analysis in ProMOS for their insightful discussion and support.

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