Study of RF Characteristic Features of Optimized SOI - MESFETs

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ABSTRACT

In previous studies we demonstrated that SOI MESFET device structure is a suitable candidate for micropower circuit applications due to its high anticipated cut-off frequency [1]. Even though the device offers higher f_T, there is no guarantee that minimum device dimension will offer optimum performance in terms of voltage gain. To examine this issue, we developed a transport model, based on the solution of the Boltzmann Transport Equation, for modeling *n*-channel silicon-on-insulator (SOI) MESFETs using the in-house Ensemble Monte Carlo device simulator. From the simulations it is observed that the optimum device exhibits 33.3GHz cutoff frequency and 25.3 voltage gain. From this analysis we may conclude that the SOI MESFET device structure is a suitable candidate for application in r.f. micropower circuit design and there exists a device structure with a particular doping, silicon film thickness and gate length that shows optimum high frequency performance in terms of cut-off frequency and voltage gain.

Keywords: Cutoff frequency, voltage gain, surface-roughness scattering, low-power r.f. applications.

1 INTRODUCTION

Micropower circuits based on sub-threshold MOSFETs are used in a variety of applications ranging from digital watches to medical implants. The principal advantage of a transistor operating in the sub-threshold regime is the minimum power consumption, but the main drawback is its speed. Micropower circuits are limited to operating frequencies below ~ 1MHz due to low cut-off frequency $f_T=\mu V_T/2\pi L_g^2$, where μ is the carrier mobility, $V_T=kT/e$ the thermal voltage and L_g is the gate length. In the sub-threshold regime, it is impractical to increase f_T by reducing the gate length because of difficulties with transistor matching. The only remaining option to increase f_T is to increase the carrier mobility. In a prototypical MOSFET device in the on state, inversion electron mobility is typically 600-700 cm^2/Vs but falls to only 100-200 cm^2/Vs in weak inversion, and one expects a cut-off frequency in the range between 40 to 80 MHz for a sub-threshold MOSFET with L_g=1 μm. For overcoming the above mentioned issues, in previous studies we already demonstrated that the SOI MESFET device structure is a suitable candidate for micropower circuit applications due to its high cut-off frequency because of the higher mobility values [1]. But from application point of view, even though the device offers higher f_T, there is no guarantee that minimum device dimension will offer optimum performance in terms of voltage gain as well. The purpose of this work is to clarify this issue.

The paper is organized in the following way. In Section 2 we discuss the methodology of the Monte Carlo technique, with emphasis on the calculation of the mobility, cutoff frequency and voltage gain. In Section 3 we present the results of our simulation experiments. We finish the paper with Section 4 in which we summarize our work and give some conclusive comments.

2 METHODOLOGY: THE MONTE CARLO METHOD

Detailed description of the Monte Carlo technique is described elsewhere [2]. Briefly, the Monte Carlo model used in the transport portion of the simulator is based on the usual Si band-structure for three-dimensional electrons in a set of non-parabolic Δ-valleys with energy-dependent effective masses. The explicit inclusion of the longitudinal and transverse masses is important and this is done in the program using the Herring-Vogt transformation [3]. Intravalley scattering is limited to acoustic phonons. For the intervalley scattering, we include both *g*- and *f*-phonon processes. The high-energy phonon scattering processes are included via the usual zeroth-order interaction term, and the two low-energy phonons are treated via a first-order process [4]. The first-order process is not really important for low-energy electrons but gives a significant contribution for high-energy electrons. The low-energy phonons are important in achieving a smooth velocity saturation curve, especially at low temperatures. The phonon energies and the coupling constants in our model are determined so that the experimental temperature-dependent mobility and velocity-field characteristics are consistently recovered [5]. In addition to phonon scattering, to properly describe the SOI MESFET devices of interest in this study, we have included surface or interface-roughness scattering in our theoretical model. In the SOI MOSFET device, carriers interact predominantly with the front Si/SiO_2 interface, and in a SOI MESFET device, they interact with the bottom Si/SiO_2 interface. It is a common practice, which we have adopted in this work as well, to include interface-roughness as a real-space scattering event, separated into diffusive and specular type of interaction with an idealized atomically-

flat interface. Specular scattering is defined as an elastic deflection by the interface where the momentum perpendicular to the interface is reversed. For the case of diffusive scattering, the deflection angle is chosen at random and utilizes uniform probability density function. In our model, 50% of the interface interactions are treated as specular and 50% as diffusive scattering [6]. Such splitting gives us low field mobility values for the Q2DEG in agreement with the experimental data. Coulomb scattering is generally associated with ionized charges in the bulk and in the SiO_2 layer, and is dominant scattering mechanism at low temperatures. For modeling Coulomb scattering, in this version of the code, we use the Brooks-Herring approach [7]. This approach accounts for the screening effect due to the rest of the mobile charges and makes the scattering potential of a short-range, rather than a long range nature.

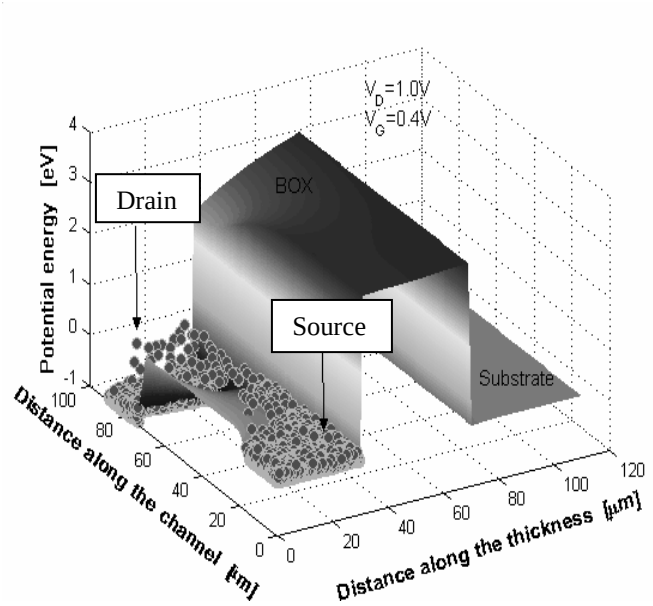

Figure 1: Two dimensional potential profiles where electrons flowing under the gate are interacting with the top interface of the BOX layer and few of them are tunneling through the Schottky barrier.

For proper inclusion of the gate tunneling and thermionic emission currents we have utilized the transfer matrix approach for linearized potentials, which leads to Airy function formulation of the problem described in details in Ref. [8]. In solving Poisson's equation, the Ensemble Monte Carlo (EMC) simulation is used to obtain the charge distribution in the device. We use the Successive-Over-Relaxation (SOR) method for the solution of the 2D Poisson equation. The Nearest-Element-Center (NEC) scheme is used as a charge assignment scheme. Within the self-consistent Monte Carlo−2D Poisson equation simulation scheme, modeling of the Schottky barrier is performed using the approach by Cowley *et al.* [9]. In the present version of the code, the Schottky barrier height is taken to be 0.656 eV to represent a $Si/CoSi_2$ material system that is used in the fabrication process of the devices being investigated in this study.

3 RESULTS AND DISCUSSIONS

Since the cutoff frequency and the voltage gain are key factors in determining device performance, it is the purpose of this study to calculate the cutoff frequency and the voltage gain by investigating the output and transfer characteristics of SOI MESFETs. To accomplish this goal, we have utilized our in-house Ensemble Monte Carlo device simulator and performed extensive simulations of SOI MESFET channels like the one shown in Figure 1.

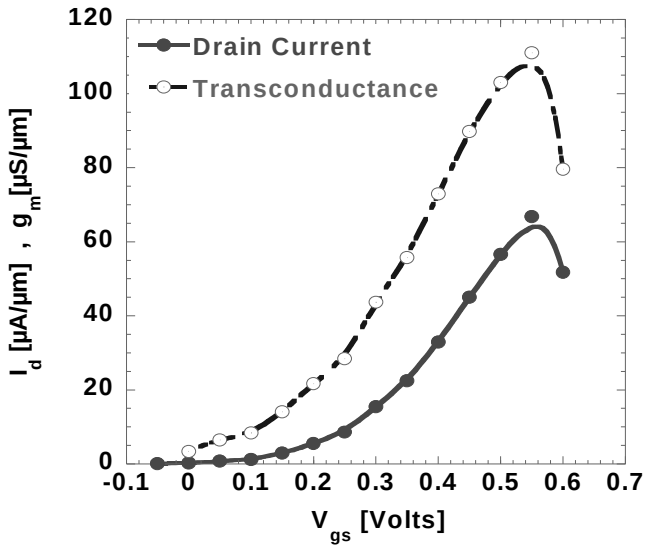

Figure 2: Transfer characteristics and variation of transconductance with gate voltage used to estimate the cutoff frequency for a particular device dimension at V_d = 0.1V.

Note that the device is going to be optimized from the application point of view if it has high cut-off frequency and high voltage gain at the same time. The cut-off frequency f_T depends on the transconductance g_m and the gate capacitance C_g. The voltage gain A_v depends on output conductance g_{out} and transconductance g_m. Thus, to optimize the performance of the SOI MESFET device structure in terms of figures of merit like the cutoff frequency and the voltage gain, a matrix of devices has been simulated using different doping densities, various SOI layer thickness and different gate lengths. A transfer characteristic for a prototypical device from the matrix with gate length Lg =50 nm is shown in Figure 2. The simulated output conductance curves are shown in Figure 3 for a particular device dimension (channel length 50 nm), where it is observed that as the drain bias increases the output conductance decreases for a particular gate bias as the slope

of the output curves reduces. The cut-off frequency f_T for each of the device structures being examined is extracted by using $f_T=g_m/2\pi C_g$, where g_m is the device transconductance and C_g is the gate capacitance. For the prototypical device from Figure 1, the extracted value of the cut-off frequency f_T is 83.6GHz and this is shown in Figure 4 (L_g=50nm t_{si} = 25nm). For optimizing the voltage gain the minimum output conductance is considered for a matrix of device structures. The cutoff frequency and voltage gain for each device structure are shown in Figure 4 and Figure 5 respectively.

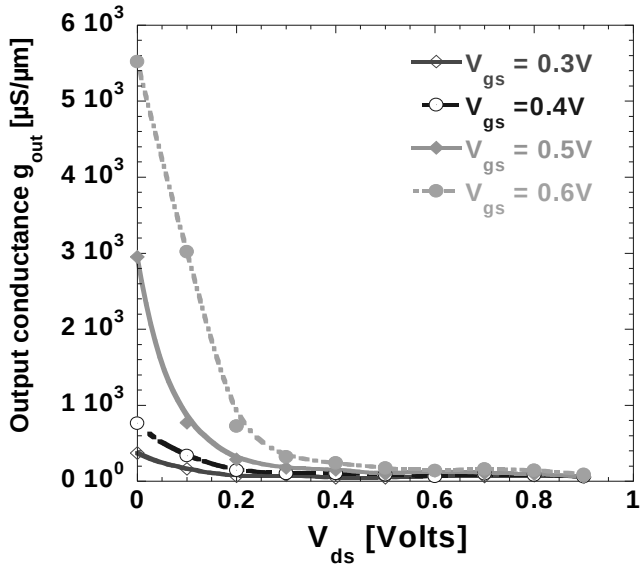

Figure 3: Output Conductance variation with respect to drain voltage for different gate voltages.

In Figure 4 the x-axis represents the gate length of the device which varies from 25nm to 100nm. The y-axis represents the simulated cutoff frequencies at two doping densities. It is observed that as the gate length reduces the cutoff frequency increases. Another feature is that the cutoff frequency increases with increase of the silicon film thickness and doping density because of the increase of the transconductance. For the device to show optimum performance the voltage gain has to be high as well. The voltage gain is found from the transconductance and the output conductance calculations. In Figure 5 it is found that voltage gain increases with the increase of gate length.

To determine which device dimension shows best performance in terms of cutoff frequency and voltage gain there are several algorithmic techniques available. In our matrix, the number of input parameters is three (silicon film thickness, doping concentration and gate length) and output parameters are two (cutoff frequency and voltage gain). Then a mathematical model is employed where the product of the cutoff frequency and the voltage gain is determined for each device from the matrix of devices we examined and the device which has maximum product is chosen to be the optimum one. From this simple model it is found that the device with a gate length of 90nm, silicon film thickness of 20nm and doping density in the channel of 5×10^{17} cm^{-3} shows optimal performance (as shown in Figure 5).

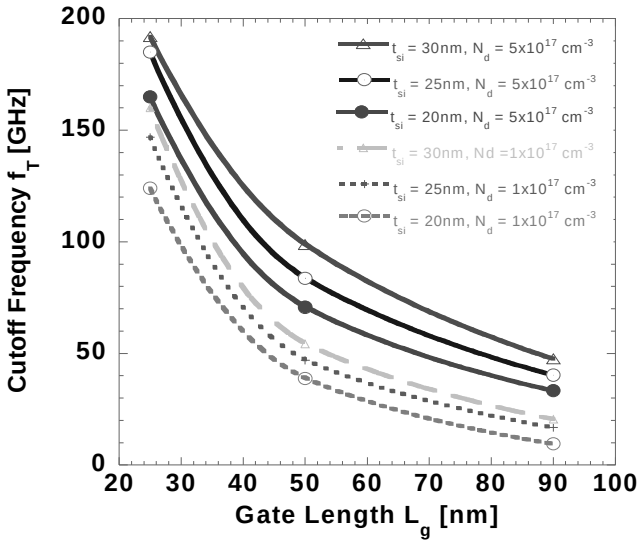

Figure 4: Cut-off frequency variation with respect to gate length for different device structures.

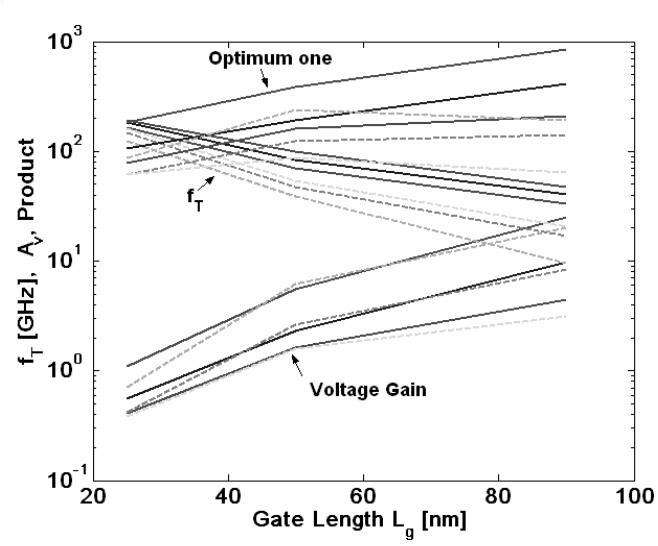

Figure 5: Determination of the optimum device dimension based on the product of cutoff frequency and voltage gain of each device structure. The doping densities are 5×10^{17} cm^{-3} (represented by the solid line) and 1×10^{17} cm^{-3} (dashed lines). The SOI layer thickness values are: 20nm (red line), 25nm (blue line) and 30nm (green line).

4 CONCLUSION

In this work, we utilized our previously developed transport model to identify optimal SOI MESFET device structure. From the simulations it is observed that the optimum device exhibits 33.3GHz cutoff frequency and 25.3 voltage gain. From this analysis we may conclude that the SOI MESFET device structure is a suitable candidate for application in r.f. micropower circuit design and there exists a device structure with a particular doping, silicon film thickness and gate length that shows optimum high frequency performance in terms of cut-off frequency and voltage gain which will be suitable not only for digital applications but also for analog applications.

5 ACKNOWLEDGEMENT

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