Fabrication and Transistor Demonstration on Si-based Nanomembranes

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ABSTRACT

We report the fabrication and demonstration of field-effect transistors (FETs) on single-crystalline, Si-based nanomembranes (SiNMs) that have thickness ranging from 40 to 250 nm. Nanomembranes such as Si, SiGe alloy, and Si/SiGe heterostructure have been released from either silicon-on-insulator (SOI) or silicon-germanium-on-insulator (SGOI) substrate by selectively removed the buried oxide layer (BOX). We demonstrate that these SiNMs can be transferred and integrated to different kinds of rigid and flexible host substrates through both wet transfer and dry printing techniques. Furthermore, by controlling the thickness and composition of Si/SiGe heterostructure, we achieved strained Si/SiGe nano-membrane via elastic strain sharing between lattice-mismatched Si and SiGe structures. DC characteristic of FETs built on these transferred SiNMs are also reported.

Keywords: elastic strain relaxation, FET, nanomembrane, SOI, SGOI

1 INTRODUCTION

Single-crystalline Si has been the most widely used semiconductor material in the very large scale integration (VLSI) era. Device performance on the bulk Si has been greatly improved over the past three decades and new substrate materials, such as SOI and strained Si on relaxed SiGe virtue substrate have been implemented to further boost the device performance [1-3]. In addition to the bulk Si, efforts on making electronic devices on single-crystalline Si-based membranes have also been made in recent years. E. Menard *et al.* reported n-type FETs on 100 nm thick microstructured Si ribbons [4, 5]. The new form of Si will potentially generate significant impact on the electronics applications where bulk Si encounters the difficulty. We report here a detailed process that could potentially be used to make very large area of single-crystalline Si, SiGe alloy, and Si/SiGe heterostructure nanomembranes. The uniqueness of this process is that one can transfer these SiNMs to any kinds of host substrates, which enables numerous possibilities of hetero-integration between high quality Si and other materials. To demonstrate capability of device fabrication on the transferred SiNMs, current-voltage curves of FETs built on Si, SiGe, and Si/SiGe nanomembranes integrated onto flexible substrate are also described.

2 FABRICATION

2.1 Nanomembrane Fabrications

To fabricate Si and Si/SiGe nanomembranes, we began with SOI as the starting material. If Si/SiGe heterostructure is desired, SiGe alloy or SiGe/Si was pseudomorphically grown on top of SOI by ultra-high vacuum chemical vapor deposition (UHV-CVD). Due to the lattice mismatch between Si and SiGe alloy, the membrane will curl into tube upon the removal of BOX layer if only SiGe was deposited on SOI substrate [6]. When a flat structure is preferred, extra Si with thickness close to that of the starting Si template layer was grown on top of SiGe alloy, which resulted in a vertically symmetric structure with SiGe alloy sandwiched by similar thickness of Si layers. Instead of curling or buckling like the asymmetric structure, the SiGe alloy relaxed through coherently stretching the top and bottom Si layers upon BOX removal until force is balanced within the tri-layer. By releasing the Si/SiGe sandwiched heterostructure, we are able to create strained Si with negligible density of dislocations [7]. The final thickness of the Si membranes and Si/SiGe sandwich structures can vary and was 140~200 nm and 200~250 nm respectively in this report. The SiGe alloy membrane, on the other hand, was released from SGOI substrate which was fabricated by wafer bonding of strained SiGe grown on Si substrate to another oxidized Si handling substrate. The Ge composition in this study is around 20 % and the template alloy layer is around 40 nm in thickness.

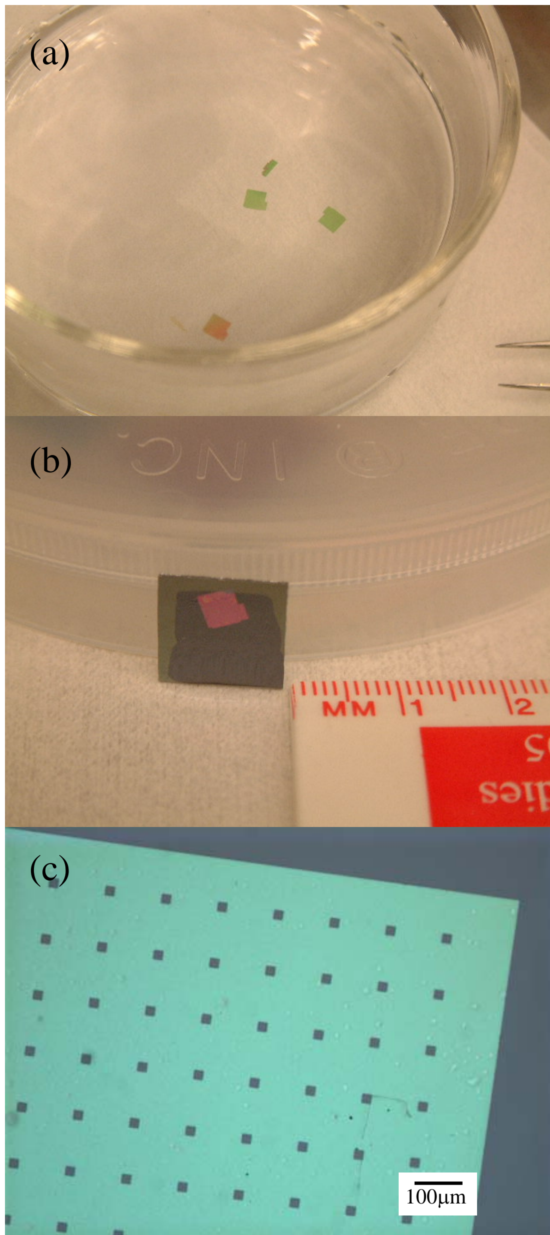

Figure 1: (a) 140 nm Si nanomembranes floating on the surface of D.I. water. (b) One of the membranes in (a) was picked up by oxidized Si host substrate and was waiting for water to dry out. The membrane dimension is around 3×3 mm^2. (c) Optical-microscopic image of a sandwiched Si/SiGe membrane on a new host substrate. Mesh holes are 20×20 μm^2 and 120 μm apart.

The release of these Si-based structures was done by selectively remove the underlying BOX layer in dilute HF. The immersion time needed to fully undercut the BOX depends on the concentration of HF and also the dimension of the releasing structures. To facilitate the release, the Si-based structures were firstly patterned into narrow strips with width of 20~50 μm or with small mesh holes distributed evenly on the structures. The mesh holes were 5 to 20 μm with separation of 120 to 200 μm so that the released membranes will have enough real-estate for devices. The patterned structures were then dry etched to the BOX layer followed by immersion into diluted HF to fully remove the BOX. The color change of the sample, due to the elimination of BOX, can sometimes be an indication of full removal. The HF was then further diluted and rinsed with D.I. water to release the membranes, which floated off onto the surface of the water where they can be easily picked up by another new host substrate. Fig. 1 shows 140 nm thick Si membranes floating on the surface of D.I. water and a close-up image of one of the floated membranes picked up by oxidized Si host substrate waiting for water to dry out. A sandwiched, symmetrical Si/SiGe membrane sitting flat on new host substrate is also shown. So far, in addition to oxidized Si, we have transferred the membranes to glass, H-terminated Si, Teflon, and metal grids using this wet transfer technique.

We have also developed an alternative dry transfer technique. In this dry transfer process, instead of floating off the membranes we printed the released membranes, which settled down on the starting SOI or SGOI handling substrate after BOX removal, face-to-face against an adhesive material. This technique works best on transferring the SiNMs onto flexible substrate and the adhesive material in this study is SU-8 series photoresist. SU-8 was spun-on ITO coated polyethylene terephthalate (PET) substrate and baked at 50ºC for 1 minute before dry transfer. After pressing the SiNMs against the SU-8, the Si handling substrate was gently peeled off and SiNMs were left on the PET substrate due to stronger bonding force between membrane and SU-8 than the van der Waal's force between membrane and Si handling substrate. Finally the entire SU-8 layer was cross-link by exposing it under UV light followed by 115ºC hard bake for 5 minutes.

Fig. 2 shows the optical-microscopic images of 200 nm Si membrane and 40 nm $Si_{0.8}Ge_{0.2}$ membrane settling down on the Si handling substrate after BOX removal (Fig. 2(a) and (b)) and the images after they were transferred onto flexible PET substrate using the dry transfer technique (Fig. (c) and (d)). The buckling of $Si_{0.8}Ge_{0.2}$ membrane on handling substrate (Fig. 2(b)) is presumably attributed to strain relaxation from the originally compressively strained alloy layer. The buckling alleviates after transferred to the PET host substrate due to the finite flow of SU-8 at elevated temperature. The Si membrane, on the contrast, stayed flat on both handling substrate and the PET host.

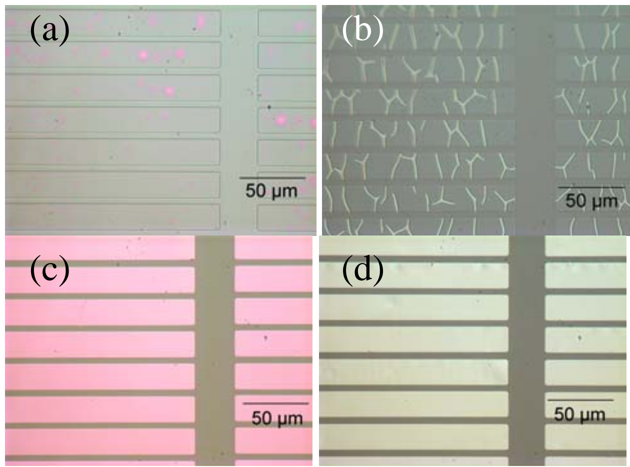

Figure 2: Optical-microscopic images of (a) 200 nm Si nanomembranes, and (b) 40 nm $Si_{0.8}Ge_{0.2}$ nanomembranes settled down on Si handling substrate after BOX removal. The membranes were patterned into 20 μm wide strips with 5 μm spacing in between. (c) Si membranes from (a), and (d) $Si_{0.8}Ge_{0.2}$ membranes from (b) that were transferred onto flexible PET host substrate by dry transfer technique.

2.2 FET Device Fabrication

For those SiNMs transferred to host substrates like oxidized Si by wet transfer technique, standard high temperature process including thermal oxidation and annealing may be applied if desired. However, it is critical to ensure good bonding between the SiNMs and new hosts before proceeds to further device processing. Without a proper bonding, the SiNMs could de-attach from the host substrates in the subsequent processing steps. We have found that by baking the sample at around 500°C for 5 minutes, we can achieve strong enough bonding force between SiNMs and oxidized Si host for device fabrication. The SiNMs stayed flat with very low density of visual defects throughout the entire high temperature device processing. In the case of strained SiNMs, depicted previously using sandwiched Si/SiGe structure, the strain shows better thermal stability on the released membrane compared with unreleased structure. It can be explained by the reduced compressive strain in the SiGe alloy due to strain sharing [8].

For those SiNMs transferred to flexible substrate by dry transfer technique, low temperature process is performed due to the incompatibility with high-temperature processing of the SU-8 and PET substrate. The FET structure that we fabricated is similar to that of the inverted-staggered thin-film transistor with the ITO coating on PET as gate electrode and the cross-linked SU-8 as gate dielectric layer. Titanium metal pads were deposited on top of the transferred SiNMs to form Schottky contact source and drain electrodes. The channel length of the FET is defined by the separation of metal pads and the channel width, in this study, is defined by the total width of the SiNMs strips that the metal pads have covered. The temperature is controlled below 120°C for the entire process. Fig. 3 shows the schematic cross-section of SiNMs FET fabricated on PET substrate. Three different SiNMs including 200 nm Si, 40 nm $Si_{0.8}Ge_{0.2}$, and 45/150/50 nm $Si/Si_{0.83}Ge_{0.17}/Si$ sandwiched structures have been transferred to PET substrate and underwent identical FET fabrication process.

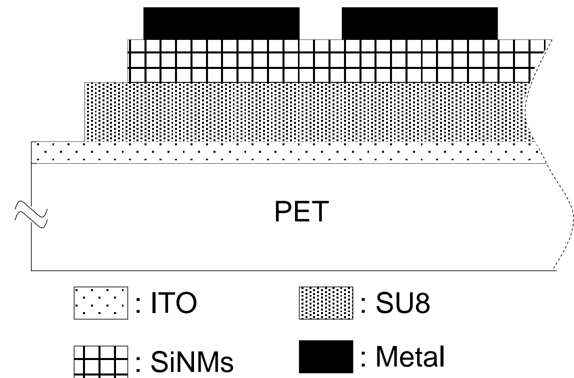

Figure 3: Schematic cross-section of SiNMs FET built on PET substrate.

3 DC MEASUREMENT RESULTS

DC measurements were performed using a HP 4155B semiconductor parameter analyzer. Fig. 4 shows the output current-voltage curves on three different SiNMs transferred onto PET substrate. The gate lengths are 3 μm and the gate widths are 60 μm in all cases. Both Si and Si/SiGe heterostructure membranes demonstrate n-type FET characteristic, while SiGe alloy membrane FET demonstrates p-type characteristic. The output current density of all three samples are limited and can be, in part, attributed to a thick dielectric layer (1.4~1.8 μm in this study) and high resistance of carriers tunneling through the Schottky barrier contacts. Much higher output current density should be achievable on the transferred membranes using thinner gate dielectric layer and ohmic contacts on doped source and drain regions.

We have evaluated the field-effect mobility on the 200 nm Si SiNM FETs using standard FET models and the extracted electron mobility was around 90 cm^2/V-sec in the linear region. The electron mobility of around 200 cm^2/V-sec was extracted using identical method on strained-Si/SiGe heterostructure SiNM FETs. The significant increase of mobility may contribute from a lower contact resistance on the Si/SiGe SiNM FETs.

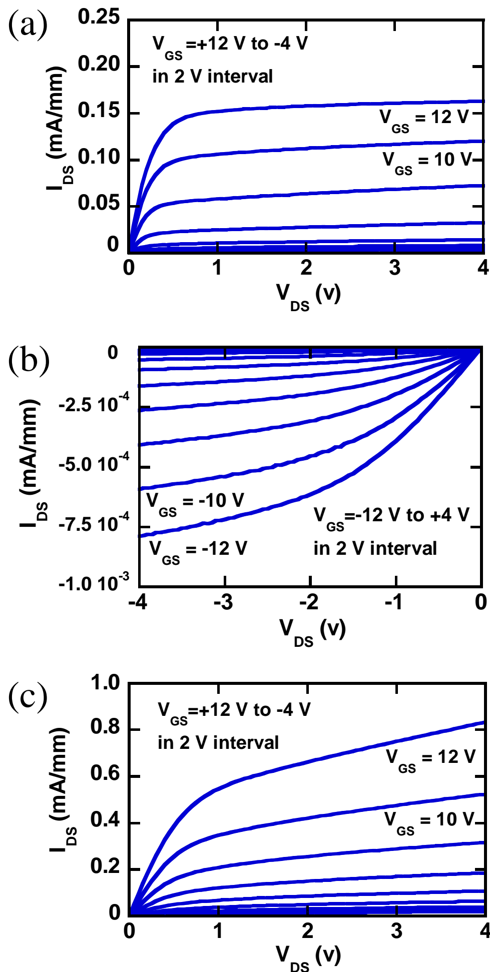

Figure 4: Output characteristic of FETs built on (a) 200 nm Si membrane, (b) 40 nm $Si_{0.8}Ge_{0.2}$ membrane, and (c) 45/150/50 nm $Si/Si_{0.83}Ge_{0.17}/Si$ membrane transferred onto flexible PET substrates.

4 CONCLUSION

Single-crystalline SiNMs can be made through the removal of BOX layer on the SOI or SGOI substrate. With the incorporation of the existing high-quality epitaxy, it is readily achievable to further engineer the strain on the membranes to obtain the desired mechanical and electrical properties. We report here the fabrication of SiNMs and the techniques to integrate them onto both rigid and flexible substrates. Though the dimension of the SiNMs is currently in tens of mm^2, we believe that these techniques can be applied to much larger area. With the capability of integrating high quality Si-based membrane with many other types of material, the study shown here opens numerous possibilities of hetero-integration. And this new integration approach could be particularly beneficial to high performance micro- and macro-electronics where a high quality semiconductor is needed.

ACKNOWLEDGEMENT

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