A Parallel Intelligent OPC Technique for Design and Fabrication of VLSI Circuit

Shao-Ming Yu and Yiming Li[1,2]

Department of Computer and Information Science, National Chiao Tung University
[1]Department of Computational Nanoelectronics, National Nano Device Laboratories
[2]Microelectronics and Information Systems Research Center, National Chiao Tung University
P.O. BOX 25-178, Hsinchu 300, Taiwan; Email: ymli@faculty.nctu.edu.tw

ABSTRACT

We in this paper develop a parallel intelligent optical proximity correction technique for process distortion compensation of layout mask. This approach integrates an improved genetic algorithm, the rule- and model-based methods, and a parallel domain decomposition algorithm to perform the mask correction on a Linux-based PC cluster with message passing interface libraries. Testing on several fundamental patterns and application to VLSI circuits, this approach shows good correction accuracy and efficiency. Benchmark results, such as speedup, and parallel efficiency are achieved and exhibit excellent parallel performance. This is a constructive approach to developing advanced computer aided design tools for design and fabrication of integrated circuits.

Keywords: OPC, lithography, genetic algorithm, parallel computing, domain decomposition, modeling and simulation, CAD

1 INTRODUCTION

Optical lithography [1-10,15] is one of key technologies used in design and fabrication of very large scale integrated (VLSI) circuits and system-on-a-chip (SoC). It transfers the desired circuit layouts onto the wafers. The exposure on wafer has distortions due to the proximity effects [3-5]. As the minimum feature sizes continue to shrink, the mismatch between the desired pattern and the actual result on wafer is significant and affects the behavior and performance of designs [3-10]. Optical proximity correction (OPC) [3-10,15] is the process of modifying the polygons that are drawn by designers to compensate for the non-ideal properties of the lithography process. Given the shapes desired on the wafer, the mask is modified to improve the reproduction of the critical geometry. Various OPC techniques have been developed, which can be grossly grouped into either rule-based or model-based. The model-based OPC [8,9,15] techniques modify whole layout by the calculations of experimental corrected models. Rule-based techniques [8,10,15] are an extension of the methods used for manual OPC which add or eliminate some defined patterns on the desired layouts to improve exposure result on the wafer. During the OPC process, lithography simulation is applied to evaluate the modified layouts. Unfortunately, whole system's lithography simulation is time-consuming and requires large computational resource.

We in this paper develop a parallel intelligent OPC technique for process distortion compensation of layout mask. It combines an improved genetic algorithm (GA) [11,12,15], the rule- and model-based methods, and static domain decomposition algorithm [13-15] to perform the mask correction on a Linux-based PC cluster with message passing interface (MPI) libraries. Application of the developed OPC prototype to fundamental patterns and different VLSI circuits shows good correction accuracy and efficiency. Parallel speedup and parallel efficiency are achieved and exhibit excellent parallel performance. This paper is organized as follows. In Sec. 2, the parallel intelligent OPC method is introduced. In Sec. 3, results and discussion are given. Finally, we draw conclusions.

2 THE PARALLEL INTELLIGENT OPC METHOD FOR LAYOUT MASK

Figure 1 shows a flowchart of the developed OPC method. First of all, an original layout is partition into several sub-domains with a parallel domain decomposition algorithm. It estimates each pattern's size and amounts of all patterns in the whole layout domain, and dispatches suitable patterns to each sub-domain. Each sub-layout is then corrected with rules [15]. Size and position for all new added patterns are optimized with respect to the calculated exposed results using the GA algorithm [15]. The exposure value is calculated with a two-dimensional lithography modeling and simulation [1-2]. After OPC procedures, each corrected layouts for all sub-domains are combined into a complete mask. To reduce the inconsistence of layout combination, there are suitable overlaps between neighbor sub-domains. When merging two neighbor sub-domains, we estimate and compare the error norm of different sub-domains in the overlaps, and then select the corrected layouts with the smaller error norms in overlaps as the final results.

Traditionally, the OPC corrected layouts are more complex than the original layouts. This approach accumulates the experience of layout, reduces the requirement of empirical knowledge for performing OPC in layout mask, and effectively achieves the rule-based correction. It is a good ideal to consider the OPC issue during designing the layouts which can not only accelerate

the OPC process but also reduce the complexity of the corrected layouts.

3 RESULTS AND DISCUSSION

Figure 2 shows one of tested fundamental patterns without applied any resolution correction. Figure 3 is the corresponding simulated exposed image of the layout shown in Fig. 2. It is found that distortions occurred between the original layout and the aerial image in each corner and the line-end shortening situation. The effect of the band limited optical system on corners is that corners become rounded on the aerial image as shown in Fig. 3. Such distortion may cause some unexpected mistake in the fabrication process. Therefore, it varies the electrical characteristics and function of designed circuits and modules. Figure 4 shows the corrected layout pattern through the developed OPC method. Figure 5 is the corresponding image which demonstrates good improvements compare with the result shown in Fig. 3. The rounded corners and line-end shorten situations are found in the figure 3. In our simulation, the contour level setting for the interface between two regions is 0.3. We apply the G-line Stepper setting where wavelength (λ) = 0.436, numerical aperture (NA) = 0.38 and coherence factor (sigma) = 0.7 in the lithography simulation. Figures 6-7 show applications of the developed OPC prototype to correction of layouts of ESD circuit and NAND gate circuit, respectively [15].

Parallelization of the developed OPC prototype is performed on our PC-based Linux cluster. Each PC is constructed with Pentium-IV 2GHz CPU, 512 MB memory, and Intel 100 MBit fast Ethernet. Figure 8 is the achieved parallel speedup and efficiency of the proposed OPC method in a large-scale layout of SoC which contains more than four thousand fundamental patterns. We find that 13 times speed is maintained and the efficiency is over 80% on the 16 CPUs cluster.

4 CONCLUSION

A parallel intelligent OPC technique has been proposed and developed for process distortion compensation of layout mask in sub-wavelength era. The rule-based technique, the model-based correction method, the genetic algorithm, and the lithography numerical simulation have systematically introduced in this work. Testing on several fundamental patterns, this approach has shown good correction accuracy and efficiency. This approach benefits the design and process flow for the fabrication of VLSI circuit and SoC.

ACKNOWLEDGEMENTS

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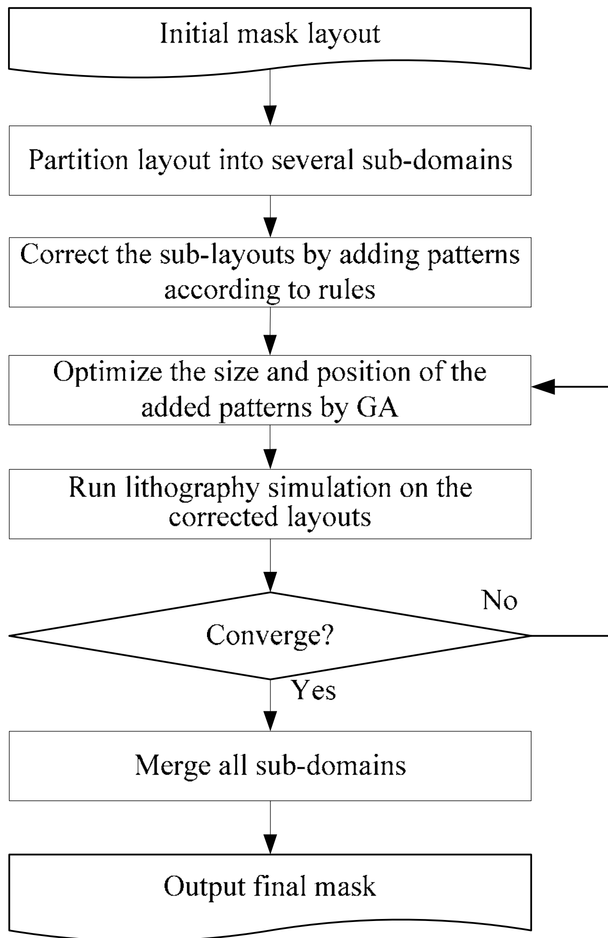


Figure 1: A flowchart of the proposed OPC method.

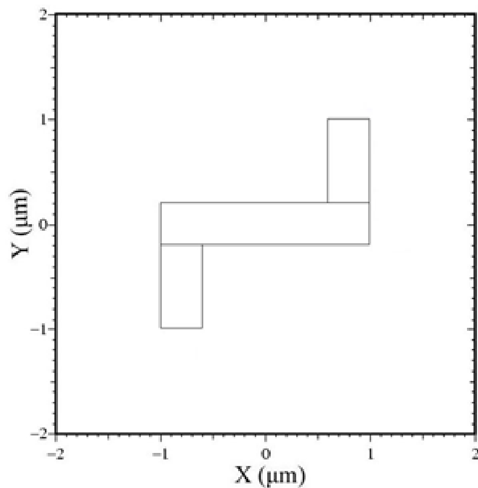


Figure 2: The tested fundamental pattern before OPC.

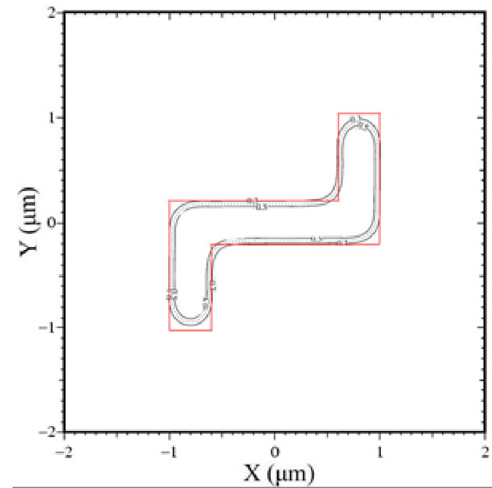


Figure 3: The simulated result of tested pattern before OPC.

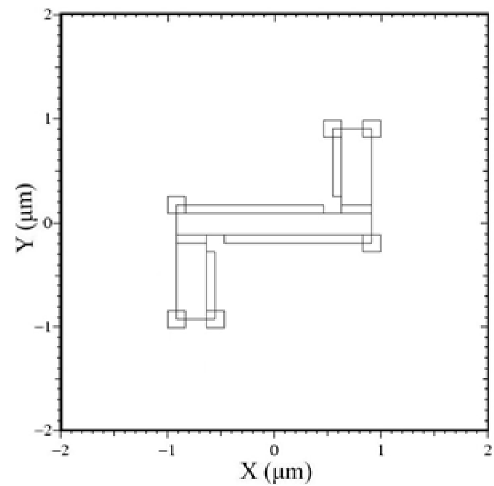


Figure 4: The tested fundamental pattern after OPC.

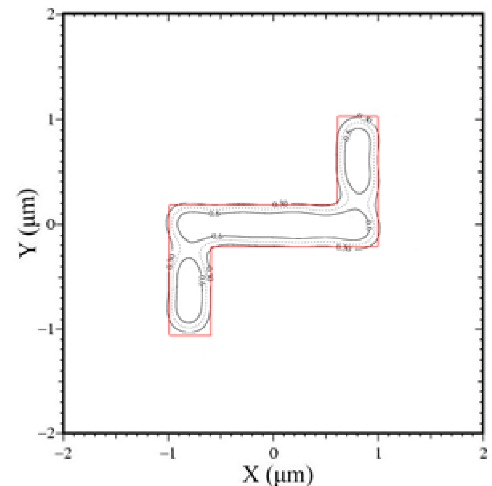
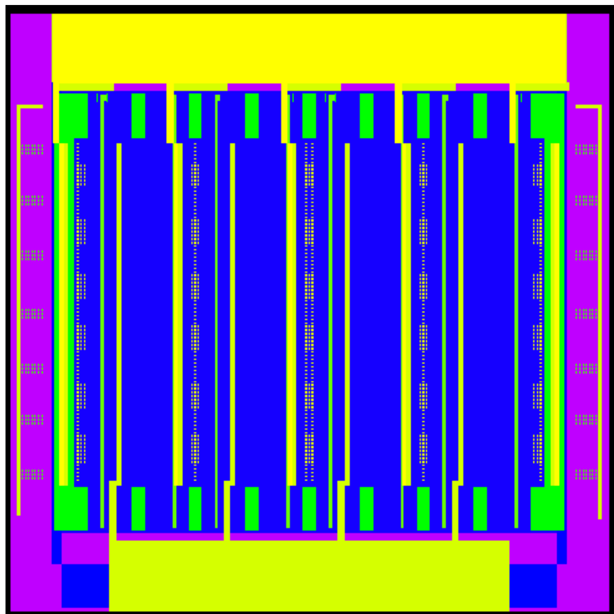
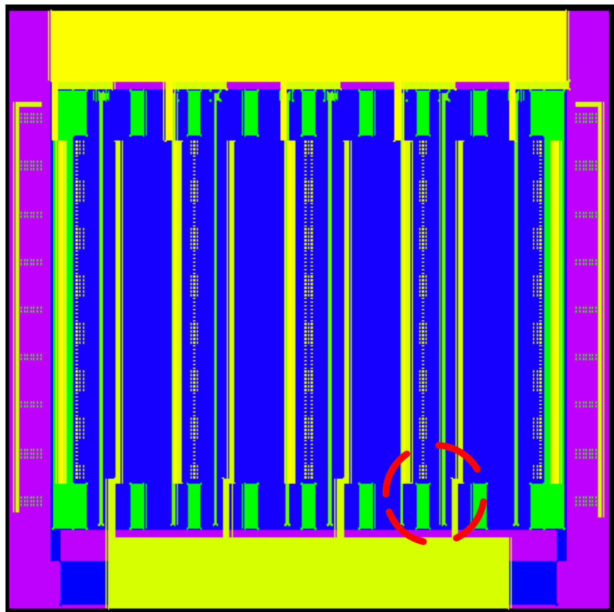


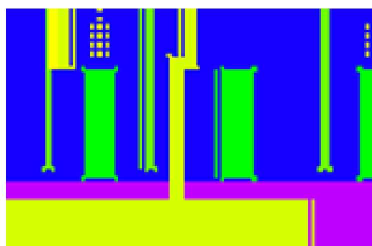
Figure 5: The simulated result of tested pattern after OPC.



(a)

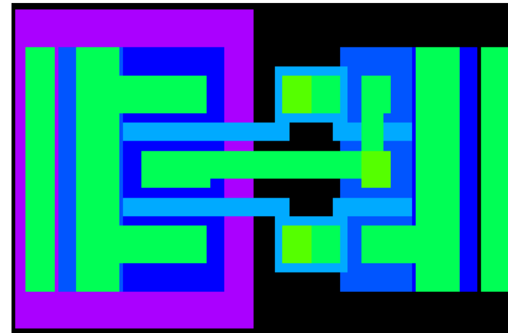


(b)

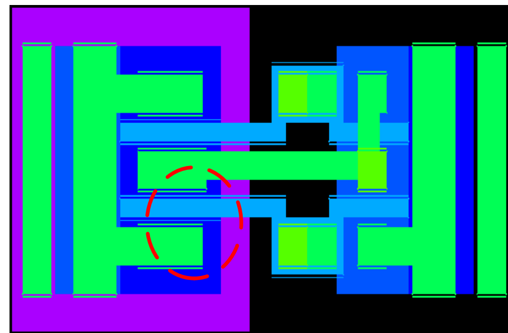


(c)

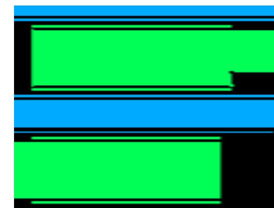
Figure 6: (a) is an ESD circuit layout, (b) is the layout corrected by the proposed OPC method, and (c) is the zoom-in plot of the circled region in (b).



(a)



(b)



(c)

Figure 7: (a) is a NAND gate layout, (b) is the corrected layout, and (c) is the zoom-in plot of the circled region.

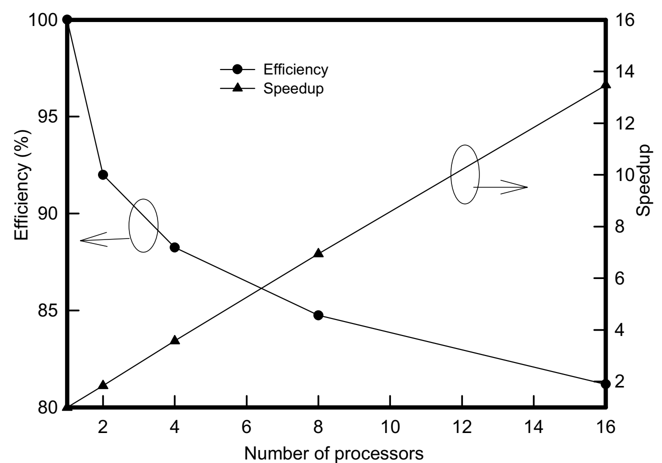


Figure 8: The achieved efficiency and speedup of the parallel computing in a VLSI layout which contains more than four thousand fundamental patterns.