A Distributed Compact Model for High-Density, On-Chip Trench Capacitors in High-Frequency Applications

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ABSTRACT

Trench capacitors integrated in a cost-effective manner into silicon for high-density decoupling capacitance applications have been fabricated and characterized. The capacitors are robust and highly linear over voltage and insensitive to temperature. A distributed model for the device is presented here. The model is computationally efficient and capable of predicting the frequency-dependence of Y-parameters.

INTRODUCTION

Despite the consolidation of electronics into chipsets for mobile applications, a large number of components are still used in discrete or co-packaged form. Improvements in cost, form-factor and reliability, and the convenience of a shorter bill-of-materials motivate the integration of these components into IC form [1-3]. A technology platform capable of achieving this must include passives such as high-Q metal-insulator-metal capacitors for coupling applications, low-T_c resistors, and high-density capacitors for supply-decoupling and bypass applications. The latter device can be built by taking advantage of the third dimension and depositing a dielectric material along the vertical sidewall of the trench (or pillar), and thereby creating capacitors in trenches [4-5].

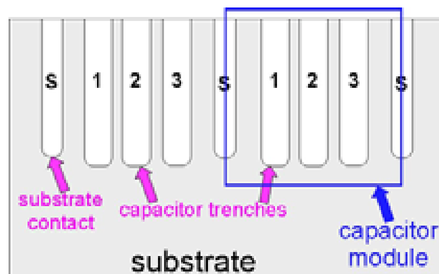

Fig. 1(a) Schematic cross-section of the trench-capacitor built and studied in this work. Designer-controlled parameters include n_f, the number of capacitor trenches between each pair of substrate contact trenches (which collectively create a capacitor "module"), and n_p, the number of modules in parallel. In the figure, n_f=3 and n_p=2.

In the past, ultra-deep trench-capacitors (100-200μm deep) have been fabricated, resulting in an effective surface area enhancement of 85x. These capacitors had a voltage dependence of about 1000ppm/V and a self-resonance frequency as low as 15MHz (the latter for a 100nF capacitor) [6-7]. We have developed and mass-produced a silicon VLSI-compatible, 7-8μm deep, ~10fF/μm^2 polysilicon-insulator-polysilicon trench capacitor with metal electrodes and deep trenches formed by reactive ion etching. Fig. 1(a) shows a cross-section of the integrated trench capacitor developed in this work: in-situ doped polysilicon is used as the bottom and top electrode in an attempt to reduce the effective series resistance and thereby improve Q. CVD-deposited silicon nitride is the dielectric of choice. The capacitance per unit area is roughly 6x higher than its planar counterpart, due to the use of trenches. The layout of the capacitor is flexible, as shown in Fig. 1(b), permitting the development and use (in circuit design) of scalable SPICE models. The periodic insertion of a top-side bottom electrode contact provides a low-resistance path to the substrate, which in some cases is moderately rather than heavily doped. The substrate contact trenches therefore have a significant impact on series resistance, and hence on Q.

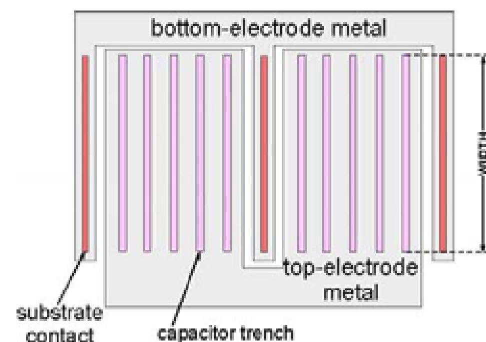

Fig. 1(b). A trench capacitor layout that permits scalability and easy incorporation into circuits. In this example, n_f=5 and n_p=2.

DISTRIBUTED SPICE MODEL

In our previous paper the RF properties of the trench capacitor were described using a lumped compact model [8]. The lumped model performs well in most situations, but requires a long measurement and extraction

process, especially when trying to describe certain high-frequency phenomena. In this paper we describe, for the first time, a distributed model for the trench capacitor, that requires fewer measurements and structures in the extraction process, and also captures high-frequency characteristics readily. The distributed model is described diagrammatically in Fig. 2 for the $n_f=2$, $n_p=1$ case. In the diagram shown, metal inductances are omitted, but may be added into the model if necessary. The vertical dimension of the trench is represented as a series of lumped elements. For the investigation, the model was coded in a flexible manner, permitting a user-defined number of vertical sections in each capacitor trench.

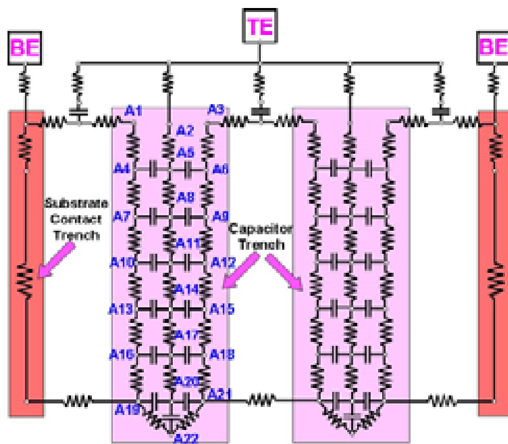

Fig. 2. Schematic representation of the distributed model for the trench capacitor, for the specific case of $n_f=2$, $n_p=1$ and $N_v=6$, where N_v is the number of vertical sections in each capacitor trench. TE represents the top metal electrode, and BE the bottom metal electrode. The circuit nodes comprising one capacitor trench are labeled for clarity.

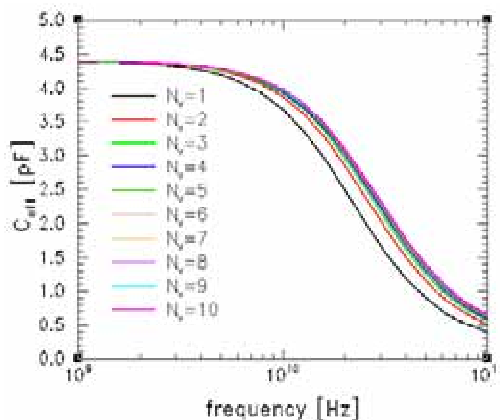

Fig. 3. Effective capacitance as a function of frequency for $n_f=2$ and various values of N_v. The curves converge for $N_v > 8$.

The substrate resistance, which can be large in some cases, is represented by the shunt-resistors connecting adjacent capacitor trenches. One can define the effective capacitance as $C_{eff}=(1/\omega)\text{Im}(Y_{11})$, with $\omega=2\pi f$. This quantity is a function of frequency, f, and is plotted in Fig. 3 for various values of N_v (and, without loss of generality, the case with $n_f=2$). Indications are that $N_v=8$ is sufficient to describe the detailed roll-off characteristics of C_{eff} in the ~GHz regime.

The effective series resistance, R_{eff}, of the capacitor is dominated by the resistance of the bottom electrode, and is therefore a function of n_f and n_p. An increase in series resistance manifests as a decrease in the corner frequency, f_c, which is given approximately by $f_c \sim 1/(2\pi R_{eff}C_{eff})$. This is borne out in Fig. 4, which is a plot of simulated C_{eff} for $n_p=1$ and various values of n_f.

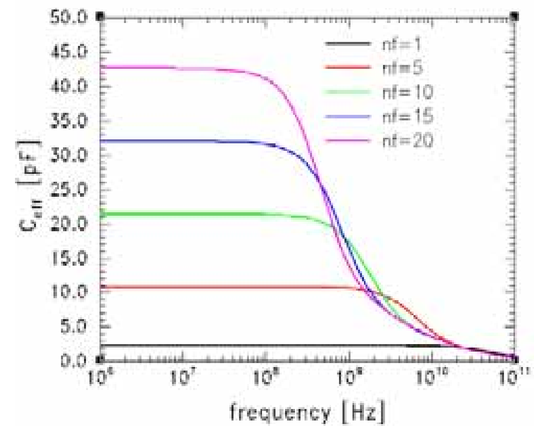

Fig. 4. Effective capacitance as a function of frequency for $n_p=1$ and various values of n_f. As n_f increases, the effective series resistance increases and corner frequency drops.

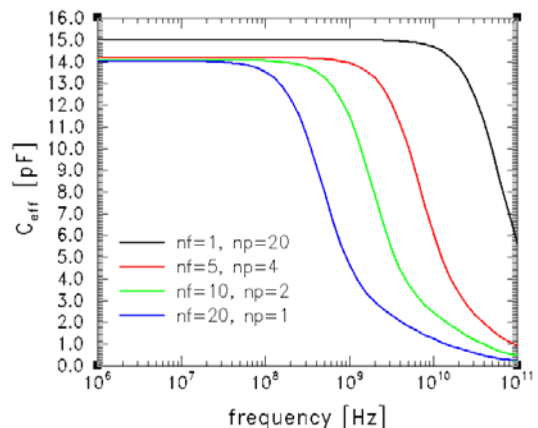

Fig. 5. $C_{eff}(f)$ for $n_f*n_p=20$ as predicted by the distributed model, for a target $C_{eff}(0)=15$pF. Increasing n_p causes a reduction in R_{eff}, which leads to an increase in f_c. The higher $C_{eff}(0)$ for $n_p=20$ is due to contributions to capacitance from planar regions of the top electrode between modules. Here W=32.92µm & $N_v=10$.

Another way to understand this effect is to fix n_p*n_f at a value that achieves a target capacitance. In this case, as in Fig. 5, the corner frequency increases with increasing n_p because of the resulting decrease in effective resistance.

For the frequencies of interest, inductance effects in the metal electrodes are negligible, because the series resistance of the polysilicon electrode dominates. Further, for widths of interest, corner and edge-effects may be ignored, when estimating polysilicon electrode resistance. That is to say, a pseudo-2D model with zero metal resistance is sufficient to predict behaviour for W > 10µm, as shown in Fig. 6. In the figure, the dots represent measured capacitance values, while the solid lines are from the distributed model. Only one fitting parameter was used in this extraction.

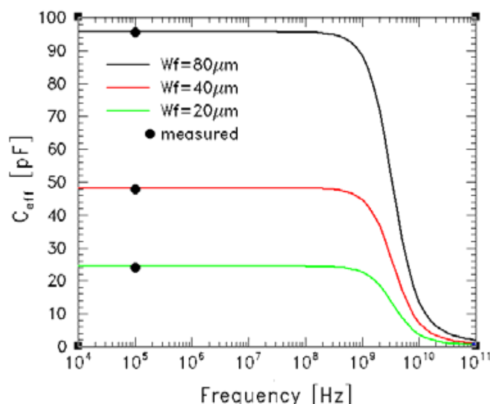

Fig. 6. $C_{eff}(f)$ for different capacitor widths. A good match between measured and simulated $C_{eff}(f=0)$ values indicates that the pseudo-2D treatment is valid for the widths under consideration.

MEASUREMENTS & MODEL EXTRACTION

Fabricated capacitors were characterized through DC and AC testing, in both two terminal and two-port (GSG) layouts. Two-terminal structures use fewer pads and can be used for DC and low-frequency, small-signal tests, while structures with GSG pads are needed for ~GHz measurements. Interconnect parasitics are removed from the measurement with the help of "open" structures.

The optimized process resulted in robust and repeatable capacitor performance. DC leakage characteristics are shown in Fig. 7: as may be expected for silicon nitride dielectrics, soft-breakdown characteristics are observed, with good uniformity across the wafer. Breakdown voltage is in the ~15V range for the dielectric thickness of the capacitors in Fig. 6. Fig. 8(a) shows the temperature dependence of $C_{eff}(f=0, V=0)$, while Fig. 8(b) shows the relatively small voltage dependence of the low-frequency capacitance. These dependencies may be quantified as $C_{eff} = C_o(n_p, n_f, f) \times [1 + \alpha(T-T_o)] \times [1+a_1V+a_2V^2]$. Here $\alpha=6.0\times10^{-3}/°C$, $T_o=0°C$, $a_1=-525ppm/V$ and $a_2=-52ppm/V^2$.

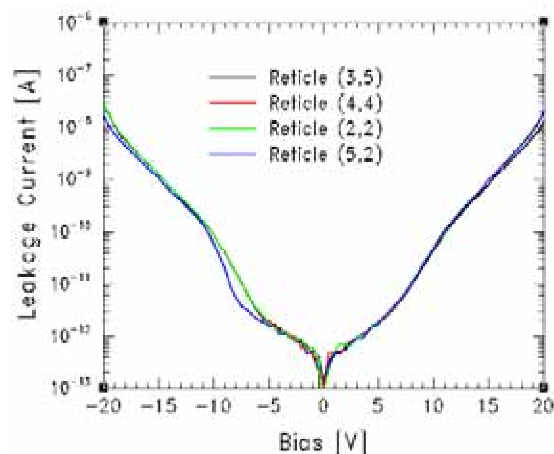

Fig. 7. Room-temperature leakage current characteristics from four locations on the wafer, with a "breakdown" voltage greater than 15V in either polarity.

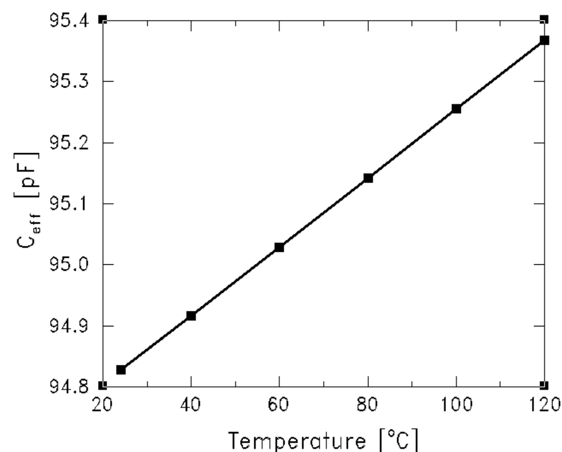

Fig. 8(a). $C_{eff}(f=0, V=0)$ as a function of temperature.

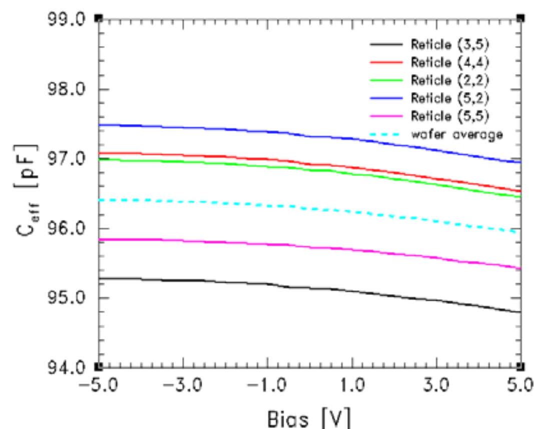

Fig. 8(b). $C_{eff}(f=0)$ as a function of voltage, showing excellent across-wafer uniformity and the extremely low voltage-dependence.

Note that in the distributed model, obtaining an analytical solution for $C_{eff}(n_p, n_f, f, T)$ is a very difficult task. The model is therefore coded into SPICE as a scalable subcircuit using N_v=10. Computational efficiency was excellent for typical circuit applications, with no perceptible increase in simulation time between an ideal, lossless, lumped capacitor and the distributed trench capacitor.

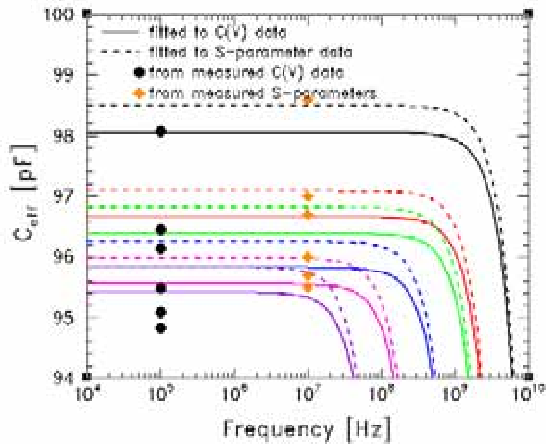

Fig. 9. $C_{eff}(f)$ for various values of n_f and n_p. Low-frequency, zero-bias measurements are included as black circles, and low-frequency capacitance derived from RF measurements as orange diamonds. For each set of data, only one parameter in the model, namely dielectric thickness, is adjusted to yield an excellent fit, with a maximum error of only 0.6%. In the plot, n_f varies from 2 to 40, with the n_f*n_p product at a constant value.

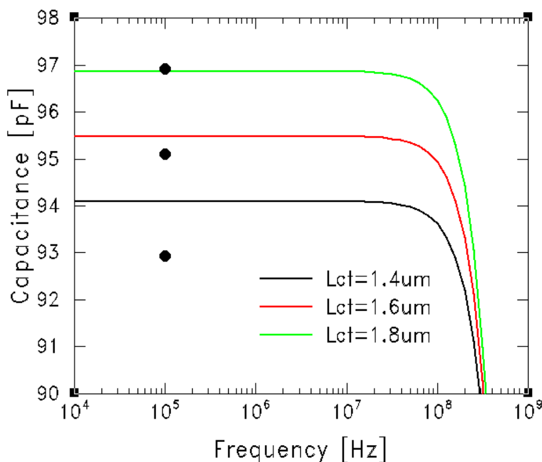

Fig. 10. $C_{eff}(f)$ for various values of L_{ct}, the capacitor trench opening, along with measured data at low frequency. Using the same model parameters as used in Fig. 9, the error in the low frequency C_{eff} is less than 1.1%.

The distributed model is based on fundamental process parameters that are derived from knowledge of layer thicknesses and sheet resistances, or are extracted from the low-frequency, zero-bias measurement of *one* or *two* capacitor geometries. As shown in Fig. 9, the model is extracted from measured data by tweaking only one parameter such as dielectric thickness, which is really the weighted average between the thickness on the planar surfaces and the thickness inside the trenches. The model is easily fitted for each set of measured data – C(V) measurements from two terminal structures and capacitance values from RF measurements. In the figure, n_f varies from 2 to 40. The maximum fitting error, found to be in the {nf=40, np=1} case, is as low as 0.6%.

Further, when the model extracted in Fig. 9 is applied without any parameter changes to capacitors with other trench opening dimensions (see Fig. 10), a good fit to the low-frequency measured data is obtained.

SUMMARY

A physically-based distributed model for integrated trench-capacitors has been developed and implemented in SPICE as a subcircuit. The model successfully predicts low- and high-frequency phenomena, and is extracted readily from the measurement of only a few devices. The model is scalable, accommodates various geometrical features and is computationally efficient for the range of applications studied.

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