Topography Simulation for Structural Analysis Using Cell Advancing Method

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ABSTRACT

In this paper, we report our proposed method for topography simulation of micro-electronic devices such as deposition and etching process. The proposed method simulates the advancement and backward movement of the surface by converting the cell structure into a tetrahedral mesh structure with topological information. The proposed scheme was verified with a test structure having 4 metal lines embedded in two types of non-planar dielectric layer and thereafter the capacitances were extracted. The simulation result exhibited about 8% maximum error, which seems to be relatively small in comparison to the one of the planar dielectric layer.

Keywords: topography simulation, deposition, etching, cell advancing method, mesh generation

1 INTRODUCTION

Despite many research efforts have been made on the development of novel schemes which allows the designer to figure out the topographical evolution of the surface during the semiconductor process such as deposition and etching, three-dimensional topography simulation is still faced with many challenges which limit the general applicability and usefulness.

A variety of surface evolution method has been studied to build a three-dimensional topography simulator; the string method, the level set method and the cell method [1-6]. The completed simulators have been used to investigate various three dimensional topography. The conventional string method sometimes causes fatal errors such as the looping of strings. The loops arise naturally at slowly etching convex corners with fast etching sides. The level set method offers quite an accurate profile for tracking interfaces despite of its inherent issue of computationally inefficiency. Furthermore, the traditional cell method has a limit because it requires intensive memory. However, the cell method has a unique feature such as the capability to easily handle the topographical evolution, adaptive meshing scheme and relatively simplicity for the extension to the three-dimension.

In this paper, we propose a cell advancing method which is different but stems from the traditional cell method for accurate topography simulation. Using the finite element method (FEM), we perform a mesh generation of the simulated topography for the calculation of parasitic capacitances.

2 TOPOGRAPHY SIMULATION METHOD

The proposed method simulates the advancement and backward movement of the surface through a list structure, so called the surface cell. Figure 1 is a schematic diagram illustrating the proposed method wherein the list constitutes a surface cell. The simulation region is supposed to be divided into units of hexahedron-shaped cells. Both the material information and the exposure information are assigned at each cell to be divided. The surface cells are constituted the list for the efficiency of the memory and computation. Figure 1(a) is a schematic diagram illustration the surface cell list composition for a surface topography expression of the case of etching. The surface cell list is composed the surface cells to be contacting with the vacuum (List1). Figure 1(b) is a schematic diagram illustration the surface cell list composition for a surface topography expression of the case of deposition. The surface cell list is composed the vacuum cells to be contacting with the surface (List2).

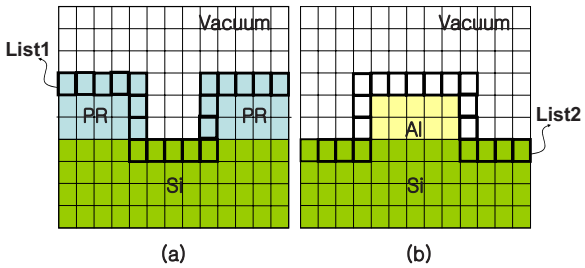

Figure 1: The cell list composition for a surface topography expression (a) the case of etching, (b) the case of deposition.

The composed surface cell list is used to do the simulation for the advancement and backward movement of

the surface. Each surface cells are moved the advancement and backward according to the total etch rate or deposition rate.

Total etch rate or deposition rate is expressed as

$$(R_x \cdot V_x + R_y \cdot V_y + R_z \cdot V_z) I(x, y, z) \qquad (1)$$

where R_x , R_y and R_z are the etch rate or deposition rate of x, y and z axis direction. V_x, V_y and V_z are the visibility of x, y and z axis direction. I(x, y, z) is the quantity of incident particle according to location of the surface cell.

Topography processes are affected by the shape of the surface. Therefore, topography simulator for deposition and etching processes are used information about incident particle distributions and the exposure information of surface. To determine the distributions of incoming particles are used the resulting particle flux distributions at a surface point. The region above the surface is divided up into several patches in a spherical coordinate system with a polar angle Θ and azimuth angle φ as shown in Figure 2.

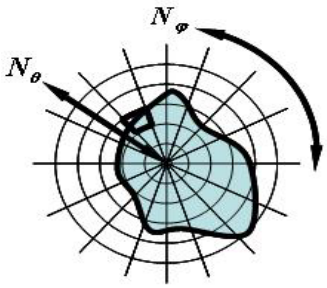

Figure 2: A top view of the hemisphere above the analysis region

Visibility expresses the exposure information of the cell about the direction for evolution. For etching and deposition process, the information about incident particle fluxes and surface reaction is employed to calculate etch or deposition rate distributions along the visibility. Figure 3 illustrates the scheme for calculating the change of visibility in accordance with the location of each cell. The C1 cell has the visibility of twice compared with the C2 cell in x axis and z axis direction. The C2 cell has the visibility by the reflection additionally.

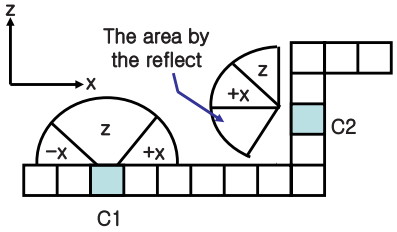

Figure 3: The change of visibility according to the location of the cell.

If, during the etch simulation, a decrement exceeds the volume value of surface cell, which is delivered at the next volume value. The error is happened more clearance than the volume of the cell in fixed time interval. We devised a spillover algorithm to solve the problem. A spillover algorithm is to remove from volume of adjacent cells to the cell with the more eliminated volume. If for example, the volume value of a give cell is 1 and the decrement is 0.2. After each time step the resulting volume value of removed cells is distributed to adjacent cells in the same direction during the etch simulation. Figure 4 shows a basic scheme of the spillover algorithm concept.

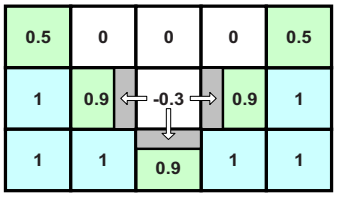

Figure 4: Basic scheme of the spillover algorithm concept.

3 MESH GENERATION METHOD

The mesh structure generation method is used the plane for the generation of layered meshes and cell height information by converting the cell structure into a tetrahedral mesh structure with topological information. Figure 5 is a schematic diagram illustrating mesh generation method. First, we acquire the height information with each cell from cell structure of the simulated topography as shown in figure 5(a). The numeric character is the height information. Same height information is combined. Figure 5(b) shows the combined cell information. The combined cell information is formed to combine the cell of the same height information. To generation the non-planer finds the height information about the node point P as shown in figure 5(c). Figure5 (d) shows the resulting triangle mesh structure.

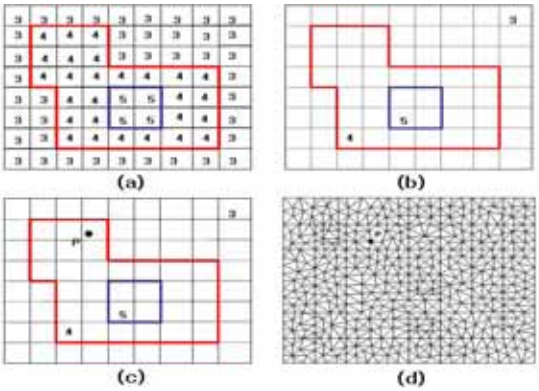

Figure 5: The method of mesh generation (a), (b) and (c) cell height information and boundary information of equivalent cells (d) triangle mesh generation.

4 SIMULATION RESULT AND DISCSSIONS

In Figure 6 is shown an example for testing the validity of the proposed scheme. The test structure has 4 metal lines which are embedded with two types of non-planar dielectric layer. The test structure is the structure which the paralleled metal lines intersects each other. The lower part metal line is embedded in the dielectric layer. The resulting upper part metal line has the non-planar shown in figure 6 (a), (b). Also the upper part metal line is embedded in the dielectric layer. The resulting lower part metal line has the non-planar shown in figure 6 (c), (d).

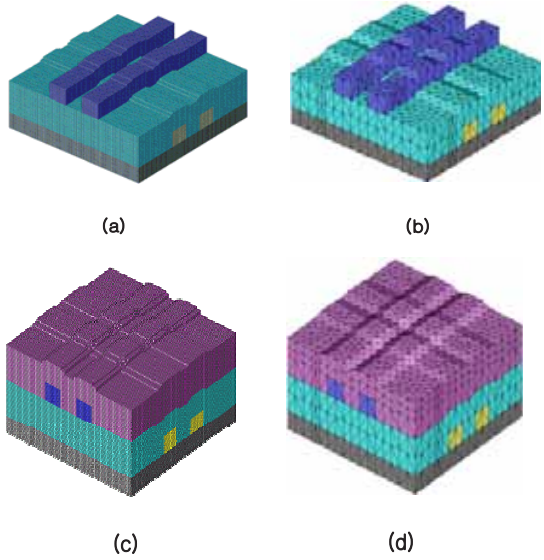

Figure 6: The case of the 2 metal lines embedded one types of non-planar dielectric layer (a) cell structure, (b) the result of a mesh generation.
The case of the 2 metal lines embedded two types of non-planar dielectric layer (c) cell structure, (d) the result of a mesh generation.

Using the generated mesh information, the parasitic capacitances are calculated between the metal lines. The parasitic capacitance is expressed as

$$C = \begin{bmatrix} \sum C_{1j} & -C_{12} & \cdot & \cdot & -C_{1N} \\ -C_{12} & \sum C_{2j} & \cdot & \cdot & -C_{2N} \\ \cdot & \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot & \cdot \\ -C_{N1} & -C_{N2} & \cdot & \cdot & \sum_{j=1}^{N} C_{Nj} \end{bmatrix} \quad (2)$$

The diagonal elements in iith are the total parasitic capacitance. The total parasitic capacitance is expressed sum of the coupling capacitance of line in ith, parasitic capacitance (C_{ii}) of between ground and between other lines. The elements in ijth express parasitic capacitance of a minus between ith line and jth line.

Table 1 provides the calculated parasitic capacitance values for the two cases wherein the non-planar is considered and not considered. The resulting values is parasitic capacitance values of the paralleled metal lines intersects each other.

	Parasitic capacitance values (pF)
The case which the non-planar plane is considered	$\begin{bmatrix} 1.513 & -0.388 & -0.194 & -0.193 \\ -0.398 & 1.518 & -0.194 & -0.194 \\ -0.194 & -0.194 & -0.505 & -0.384 \\ -0.193 & -0.194 & -0.384 & -1.504 \end{bmatrix} \times 10^{-3}$
The case which the non-planar plane is not considered	$\begin{bmatrix} 1.491 & -0.397 & -0.178 & -0.178 \\ -0.317 & 1.491 & -0.178 & -0.178 \\ -0.178 & -0.178 & 1.491 & -0.178 \\ -0.178 & -0.178 & -0.403 & 1.472 \end{bmatrix} \times 10^{-3}$

Table 1: This table shows parasitic capacitance values of the case which the non-planar is considered and not considered.

The simulation result exhibited about 8% maximum error, which seems to be relatively small in comparison to the one of the planar dielectric layer. The change of such parasitic capacitance is altered according to the form of the non-planar. The influence about the non-planar must consider consequently.

Several topography simulation results demonstrate the proposed cell advancing method.

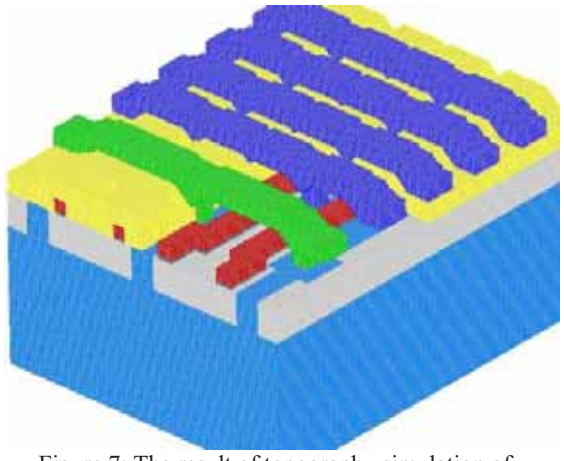

Figure 7: The result of topography simulation of a ROM structure.

Figure 7 shows three-dimensional topography simulation of a ROM structure. This resulting is a final profile structure on the wafer after topography simulation in accordance with the user-defined layout and process procedure. According to the proposed cell advancing method, simulation region is divided into units of hexahedron-shaped cells. The simulation region is used the size 452 μm × 156 μm × 8 μm. This structure has total 426,400 (104 × 50 × 82) cells. The generated structure converts triangle mesh structure to calculate the parasitic capacitance. To calculate the parasitic capacitance must be considered the influence by the non-planar. This ROM structure has many non-planar as shown in figure 7. This structure takes the influence by the non-planar much more. Consequently the structure must consider the form of the non-planar.

Figure 8 shows the simulation result for the PVA structure of TFT-LCD. This resulting is simulated with the proposed cell advancing method. The liquid crystal cell is taken the influence of the characteristic of non-planar. Therefore the liquid crystal cell must consider about the characteristic which appears consequently in the non-planar. But the case of the TFT-LCD has about 270 μm × 90 μm which is the ranges to XY plane. The thickness of the top and bottom is approximately 6 μm including the liquid crystal and electrode. Especially, the thickness of the electrode is less than 0.1 μm. Therefore the non-planar must consider about the case of the 0.1 μm which is the thickness. If the minimum cell size is assumed 0.1 μm. The number of cells is 2700 × 900 × 60. The resulting memory is need not more than 500Mbyte to store the information of the cells. The memory is desired efficient management method.

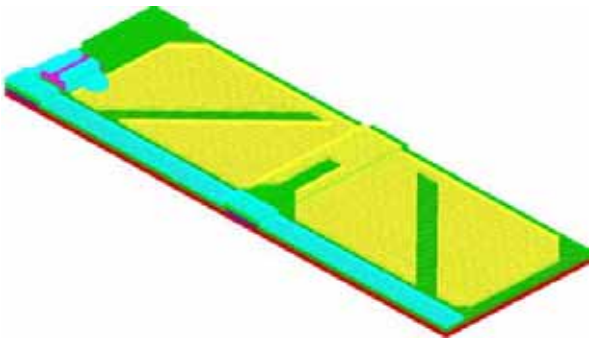

Figure 8: The result of topography simulation of a PVA mode liquid crystal cell.

5 CONCLUSION

In conclusion, we report a novel topography simulation scheme for numerical analysis of complex device structure. The proposed method guarantees computational efficiency with affordable memory size due to efficiency in implementing the cell list. The proposed scheme was employed for the calculation of parasitic capacitance values of a test structure having 4 metal lines embedded with two types of non-planar dielectric layer. The simulation result exhibited approximately 8% maximum error compared to that of planar dielectric layers. It is considered that the cell advancing method is very suitable to figure out the profile during the deposition/etching process of nano-scale processes.

6 ACKNOWLEDGEMENT

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