Three-Dimensional Transient Electro-Thermal Interconnect Simulation for Stress and Electromigration Analysis

S. Holzer*, Ch. Hollauer**, H. Ceric**, S. Wagner*, R. Entner*
E. Langer**, T. Grasser*, and S. Selberherr**

* Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics
Gußhausstraße 27–29, A–1040 Wien, Austria, holzer@iue.tuwien.ac.at
** Institute for Microelectronics, Vienna University of Technology

ABSTRACT

We introduce the coupling of three-dimensional transient electro-thermal interconnect simulations with intrinsic thermo-mechanical stress solutions. In order to study the development of local thermal stresses we use a finite element simulator for the investigation of complex layered interconnect structures at different operating conditions. The obtained local stress, temperature distribution, the current density, and the potential distribution represent the complete input data for accurate electromigration analysis.

Keywords: three-dimensional interconnect simulation, transient simulation, electro-thermal simulation, thermal stress investigation

1 INTRODUCTION

The steady enhancements of state-of-the-art integrated circuit designs have shown that interconnect structures are becoming a dominant factor for determining the system performance. Interconnect reliability is reduced due to the evolution of thermal induced mechanical stress in addition to the intrinsic stress of the material. Thus, the vacancy distribution increases and therefore, electromigration has become a serious design issue especially for long interconnect lines.

Experimental results indicate that Joule heating has a strong impact on the magnitude of the maximum allowed temperature of the global lines, despite negligible changes in the chip power density [1]. High temperature gradients in interconnect structures are known as a significant electromigration promoting factor [2]. Additionally, the thermal volume expansion mismatch between the metal and the passivation layers causes mechanical stress which is an important reason for raising electromigration failures [3], [4].

The confinement of the metal lines by its barrier and passivation layers is essential in controlling the characteristics of the thermal stresses and their relaxation behavior. With decreasing line dimensions the confinement effect is enhanced and the stress level increases significantly which causes a higher vacancy distribution and increases the probability of void formations [5], [6].

2 ELECTRO-THERMAL MODEL

The three-dimensional electro-thermal problem with self-heating for three dimensions is described by the heat conduction equation, the power loss equation, and the Laplace equation [7], [8]

$$\operatorname{div}(\gamma_{\mathrm{T}} \operatorname{grad} T) = c_{\mathrm{p}} \rho_{\mathrm{m}} \frac{\partial T}{\partial t} - \rho, \quad (1)$$

$$\rho = \gamma_{\mathrm{E}} \| \operatorname{grad} \varphi \|^2, \quad (2)$$

$$\operatorname{div}(\gamma_{\mathrm{E}} \operatorname{grad} \varphi) = 0. \quad (3)$$

γ_{T} denotes the material specific thermal conductivity, γ_{E} the electrical conductivity, ρ the electrical power loss density, c_{p} the specific heat, and ρ_{m} the mass density.

For the conductivities of the different materials a second order polygonal model is used [8]:

$$\gamma(T) = \frac{\gamma_0}{1 + \alpha(T - T_0) + \beta(T - T_0)^2}. \quad (4)$$

The structure of this formula is used for both the electrical conductivity $\gamma_{\mathrm{E}}(T)$ and the thermal conductivity $\gamma_{\mathrm{T}}(T)$ correspondingly, where γ_0 is the conductivity at the reference temperature $T_0 = 300\mathrm{K}$, α denotes the first order temperature coefficient, and β the second order coefficient.

The temperature-dependence of the heat capacitance $c_{\mathrm{p}}(\tau)$ is modeled with the Shomate equation [9]:

$$c_{\mathrm{p}}(\tau) = A + B\tau + C\tau^2 + D\tau^3 + \frac{E}{\tau^2} \quad (5)$$

where $\tau = T/1000\mathrm{K}$ represents the normalized temperature.

As a solution from the transient electro-thermal simulation we obtain the temperature distribution in the interconnect lines, in the barrier layers, and in the passivation layers. This resulting temperature distribution is used to set up the thermo-mechanical problem.

NSTI-Nanotech 2005, www.nsti.org, ISBN 0-9767985-2-2 Vol. 3, 2005

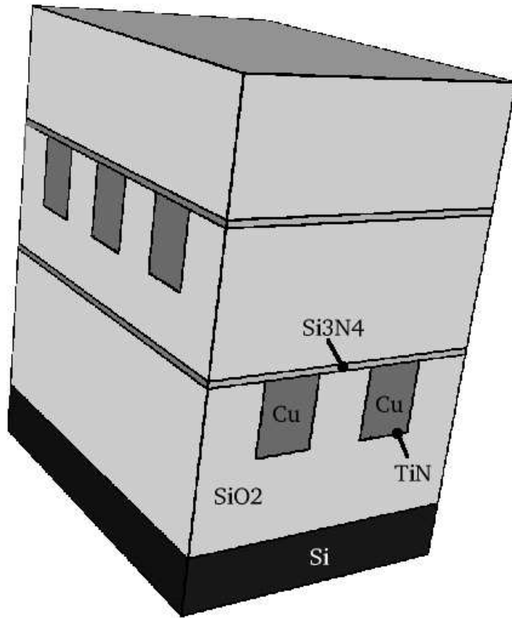

Figure 1: Typical interconnect structure consisting of several layers.

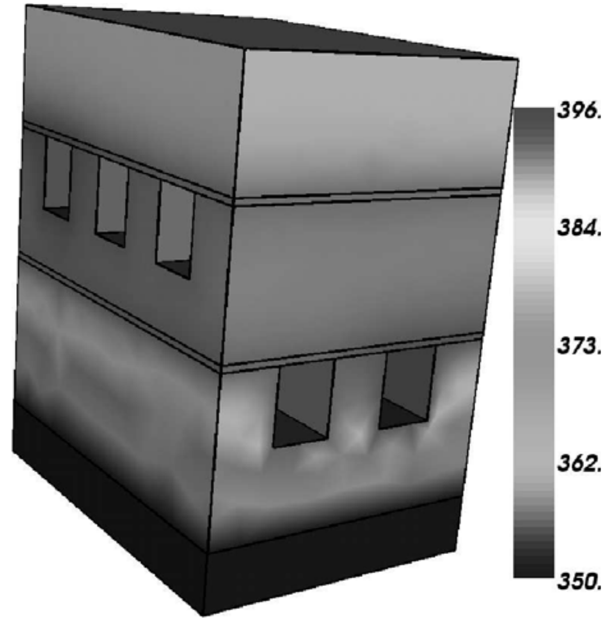

Figure 2: Temperature distribution [K] in the barrier and passivation layers.

3 THERMO-MECHANICAL MODEL

The temperature-dependent mechanical model describes the local volume expansion due to the increase of the local temperature. Since the different local element expansions result in a local stress distribution due to the confinement by the barrier and passivation layers.

The equations for the stress development due to the thermal expansion are

$$\sigma_{ij}(T) = B\alpha(T - T_0)\delta_{ij} + \lambda\varepsilon_{kk}\delta_{ij} + 2\mu\varepsilon_{ij}, \quad (6)$$

$$\varepsilon_{ij} = \frac{1}{2}\Big(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\Big), \quad (7)$$

$$\mathrm{grad}\,\tilde{\sigma} = 0. \quad (8)$$

where B denotes the bulk modulus, α the thermal volume expansion coefficient, μ and λ the Lame constants, ε_{ij} the components of the strain tensor $\tilde{\varepsilon}$, $\vec{u}$ the local displacement vector, $\vec{x}$ the position, and $\tilde{\sigma}$ the stress tensor.

The equation system consisting of the equations (1)-(3) for the electro-thermal model together with the equations (6)-(8) for the thermo-mechanical model describes the time-dependent evolution of the temperature and the corresponding hydrostatic stress distribution in the interconnect structures [10].

For the multi-layered interconnect structure shown in Figure 1 the electro-thermal equation system (1)-(3) is solved numerically and we obtain the temperature distribution in the SiO_2 and Si_3N_4 layers, which is depicted in Figure 2. Based on that result and the thermo-mechanical equations from (6)-(8) we can determine the stress distribution as shown in Figure 3.

4 SIMULATION RESULTS

The electro-thermal simulation has been performed with the three-dimensional interconnect simulator Stap from Sap [11], [12] (Smart Analysis Programs) in the transient electro-thermal mode. The simulation step afterwards for the local stress analysis has been performed with the stress calculation module of the three-dimensional Fedos (Finite Element Diffusion and Oxidation Simulator). We investigated the interconnect structure shown in Figure 1 in which the copper interconnect lines are embedded in SiO_2 and Si_3N_4 passivation layers. The lower and the upper interconnect lines are connected with vias. These vias consists also of copper and the corresponding barrier and passivation layers. On the bottom is a silicon substrate at a constant temperature of 350 K, which is used as a heat sink [13]. Between the lower layer and the upper layer interconnect lines we have a voltage applied which is switched on at the beginning of the simulation time ($t = 0$). We obtain the temperature distribution of the complete structure by a transient simulation which is mainly determined by self-heating of the interconnect lines. Therefore, the temperature change in the copper lines is negligible and

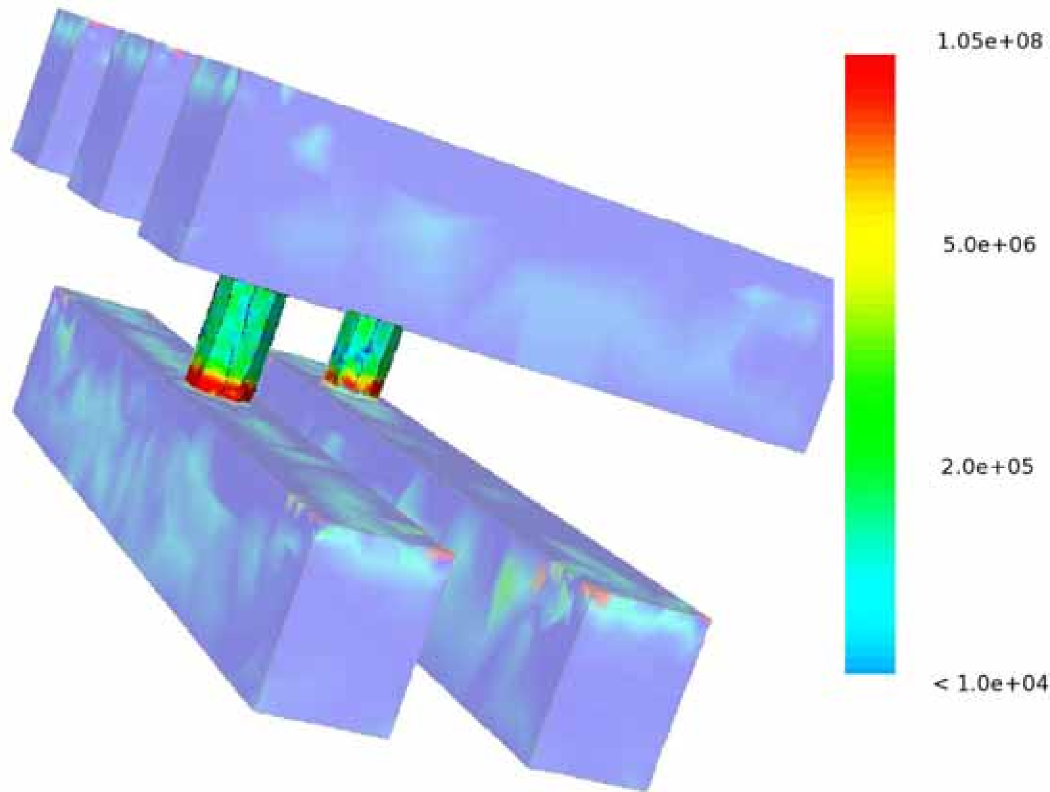

Figure 3: Pressure distribution [Pa] in the copper interconnect lines, the barrier layers, and the vias.

the set of the heated lines can be assumed to be a distributed single heat source due to the high thermal conductivity of the copper interconnect lines in comparison to the surrounding materials. The temperature gradient in the barrier layer between the copper regions in the via is almost negligible. However, for further investigations, especially for the stress analysis, it is necessary to provide this information.

The structure has been separated into two parts for an accurate visual investigation. The material compound is split into two major parts: the interconnect part with the stress distribution as shown in Figure 3 and a part with the dielectric materials with the temperature distribution as shown in Figure 2. Thus, those parts which show a critical stress level can be easily indentified and extracted for more accurate investigations and optimization purposes.

The main design issue for the part with the interconnect line is the thermal stress distribution due the internal temperature gradient and the corresponding volume mismatch between the lines and their passivation and barrier layers. For the dielectric materials the main issue is the local temperature indicating the most heated regions which can cause dielectric breakdown.

For investigation on the critical parts like vias and edges as shown in Figure 4 there can be seen a typical current path, where the stress shows a maximum.

In Figure 4 the current flows from the lighted right upper region to the bottom perpendicular from the drawing layer in direction to the viewer.

Between these two regions there are areas of relatively low stress, which correlate directly with the local current density distribution in the via.

Together with the potential distribution and the corresponding current density distribution we have the complete input parameter set for electromigration analysis available.

5 CONCLUSION

We coupled fully three-dimensional transient electrothermal simulations with fully three-dimensional thermomechanical stress simulations, which allows us to provide appropriate input data for electromigration analysis in three dimensions. The results in Figure 3 and 4 show that the peak value of the pressure is generated at the bottom of the copper interconnect vias, which highlights these areas as the ones with the highest risk of

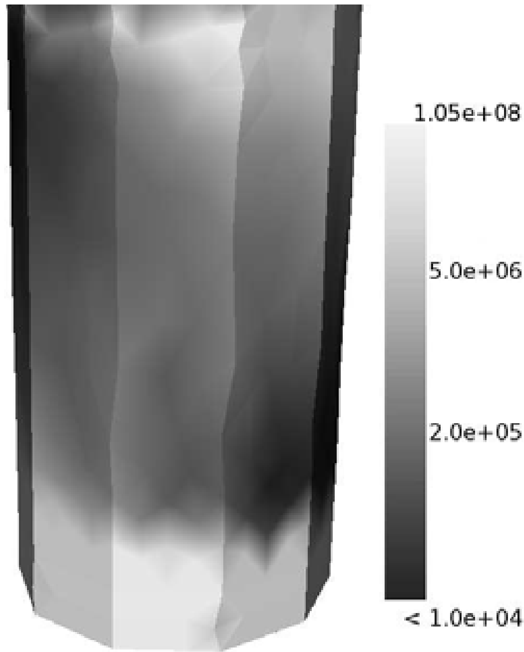

Figure 4: Pressure distribution [Pa] in the most stressed via.

electromigration. In addition, these results give information about the locally stressed regions in the dielectric materials, which can be used for further reliability investigations on the life time of these materials.

The results of this work show the significance of accurate simulation in the coupled electro-thermal regime as well as in the thermo-mechanical regime which is necessary to get reasonable results for the time-dependent evolution of the local stress.

Both type of regions, the vias and the edges of the interconnect are highly stressed due to the intrinsic temperature increase during operation, because the barrier and the passivation have a smaller volume expansion coefficient than copper and these materials can not be instantaneously brought to a certain temperature.

With these results we are able to obtain the necessary input data not only for the intrinsic stress but also for the exogenously induced stress which causes a higher vacancy distribution and therefore a higher probability for void formation.

ACKNOWLEDGMENT

This work has been partly supported by the Europaen Commission, project MULSIC, IST-2000-30133 and PROMENADE, IST-2002-2312.

REFERENCES

[1] K. Banarjee and A. Mehrotra, "Coupled Analysis of Electromigration Reliability and Performance in ULSI Signal Nets," *Proc. 2001 International Conference on Computer-Aided Design*, pp. 158–164, 2001.

[2] R. Kircheim, "Stress and Electromigration in Al-Lines of Integrated Circuits," *Acta Metallurg. ET Mater.*, Vol. 40, no. 2, pp. 309–323, 1992.

[3] X. Yu and K. Weide, "A Study of the Thermal, Electrical, and Mechanical Influence on Degradation in an Aluminum-Pad Structure," *Microelectron. Reliab.*, Vol. 37, No.10–11, pp. 1545–1548, 1997.

[4] D. Dalleau and K. Weide-Zaage, "Three-Dimensional Voids Simulation in Chip Metallization Structures: A Contribution to Reliability Evaluation," *Microelectron. Reliab.*, Vol. 41, No. 9–10, pp. 1625–1630, 2001.

[5] H. Ceric and S. Selberherr, "An Adaptive Grid Approach for the Simulation of Electromigration Induced Void Migration", *IEICE Transactions on Electronics*, pp. 421–426, 2003.

[6] H. Ceric and S. Selberherr, "Simulative Prediction of the Resistance Change due to Electromigration Induced Void Evolution", *Microelectron. Reliab.*, Vol.42, No. 9–11, pp. 1457–1460, 2002.

[7] C. Harlander, R. Sabelka, R. Minixhofer, and S. Selberherr, "Three-Dimensional Transient Electro-Thermal Simulation," in *5th THERMINIC Workshop*, (Rome, Italy), pp. 169–172, Oct. 1999.

[8] S. Holzer, R. Minixhofer, C. Heitzinger, J. Fellner, T. Grasser, and S. Selberherr, "Extraction of material parameters based on inverse modeling of three-dimensional interconnect fusing structures", *Microelectronics Journal*, Vol. 35, no. 10, 2004.

[9] A.Cezairliyan, "Specific heat of solids", Hemisphere Publiching Corp., 1988.

[10] C. Hollauer, S. Holzer, H. Ceric, S. Wagner, T. Grasser, and S. Selberherr, "Investigation of Thermo-Mechanical Stress in Modern Interconnect Layouts", in *Proc. 6th International Congress on Thermal Stresses*, 2005.

[11] R. Sabelka, "A Finite Element Simulator for Three-Dimensional Analysis of Interconnect Structures", *Microelectronics Journal*, Vol.32, No.2, 2001, pp. 163-171.

[12] IμE, *The Smart Analysis Programs - User's Manual for Version 2.9*, Institut für Mikroelektronik, Technische Universität Wien, Austria, 2003.

[13] R. Sabelka, *Dreidimensionale Finite Elemente Simulation von Verdrahtungsstrukturen auf Integrierten Schaltungen.* Dissertation, Technische Universität Wien, 2001.