Examination of the Effects of Unintentional Doping on the Operation of FinFETs with Monte Carlo Simulation Integrated with Fast Multipole Method (FMM)

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ABSTRACT

Novel device structures such as dual gate SOI, Ultra thin body SOI, FinFETs, etc. have emerged as a solution to the ultimate scaling limits of conventional bulk MOSFETs. In this paper, we use a semi-classical 3D Monte Carlo device simulator to investigate important issues in the operation of FinFETs. Fast Multipole Method (FMM) has been integrated with the EMC transport kernel to enhance the simulation time. Fin extension length on each side of the gate plays an important role in controlling the device behavior. It is found from the simulation that the presence of single unintentional dopant in the lightly doped or undoped channel has significant effects on device performance particularly near subthreshold regime. Also impurities at the source end of the channel are found to have most significant impact on the device performance.

Keywords: FinFET, Unintentional doping, FMM.

1 INTRODUCTION

Scaling of conventional bulk-MOSFETs is approaching physical limits due to the upper limit imposed on the oxide thickness, S/D junction depth, etc. As channel length shrinks below 50 nm [1], complex channel profiles are required to achieve desired threshold voltage and to alleviate short channel effects [2]. The double gate MOSFET has been proposed as a promising structure [3] for future technology. With two gates controlling the entire fully depleted channel film, Short Channel Effects (SCE) can be greatly suppressed. Among different double gate devices, FinFET is found to show better performance. FinFET is attractive to researchers due to its quasi planar structure, better immunity to SCEs, higher drive current without reducing oxide thickness or gate length and good area efficiency compared to other double gate structures [4].

Figure-1 depicts the geometry of FinFET being simulated. It consists of vertical channels formed in opposite faces of *Si* fin controlled by self-aligned double gate [5-7]. The fin height, when compared to bulk MOSFET, represents the channel width of a single-fin transistor. The fin is usually intrinsic or lightly doped to avoid channel dopant fluctuation and threshold voltage sensitivity to fin width. n^+ polysilicon gate has been assumed as a gate electrode.

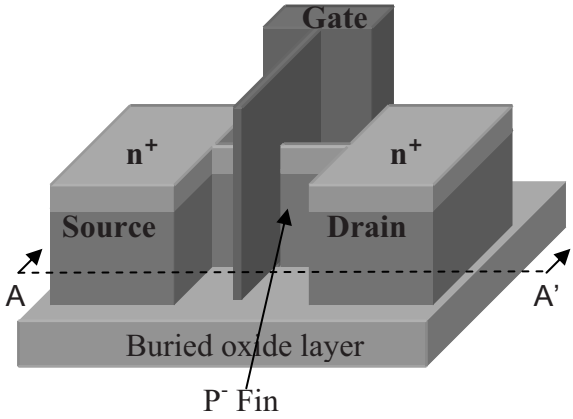

Figure 1: 3D schematic view of FinFET.

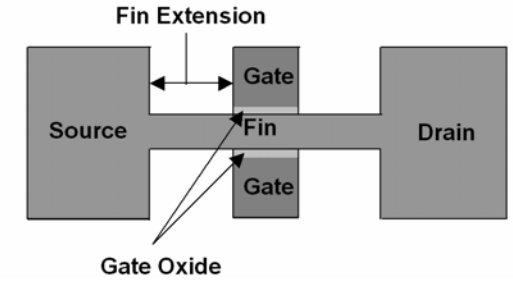

Figure 2: Top view of the FinFET shown in Figure 1 across plane A-A'.

2 SIMULATION METHODOLOGY

In our existing Poisson-EMC simulator, short-range electron-electron and electron-ion interactions are included using P^3M approach. Intravalley scattering is limited to acoustic phonons. For intervalley scattering we have included both g and f phonons [8]. We have used Incomplete Lower Upper (ILU) decomposition method to solve 3D Poisson equation. However, the charges obtained from the EMC simulation are usually distributed within the

continuous mesh cell instead of on the discrete grid points. The Particle Mesh (PM) method is used to perform the switch between the continuum in a cell and discrete grid points at the corners of the cell. NEC (Nearest Element Center) scheme has been adopted for that purpose.

Fast Multipole Method (FMM) [9] which we have utilized in this work, is a novel approach to evaluate all interactions of an N body system with CPU time requirements of order $O(N)$. Direct evaluation requires $O(N^2)$. The complexity of particle-in-cell methods is of the order of $O(N+M\log M)$, where M is the number of mesh points. In FMM-EMC scheme the time consuming Poisson equation is solved only once at the very beginning of the simulation to take into account the boundary condition. Afterwards in successive cycles FMM [10] is called iteratively to calculate both long-range and short-range e-e and e-ion interactions. The resultant force is then applied to drift the carriers. The basic idea behind FMM algorithm is to use *Multipole expansion* [9] to determine the potential V (MKS unit) due to a collection of charges as given below [11]

$$V = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{i=0}^{\infty}\frac{1}{R^{i+1}}\int r^i P_i(\cos\varphi)\rho(r)d^3r\,, \qquad (1)$$

where $P_i(x)$ is the Legendre polynomial of degree i and R is the distance from the origin to the observation point and $\rho(r)$ is the charge density. This corresponds to a series expansion of charge density $\rho(r)$ in terms of its moments, normalized by the distance to a point R far from the charge distribution. The *multipole moment* associated with a distant group can be translated into the local coefficient of the expansion associated with a local group. Interactions with particles, which are nearby, are handled directly. The discontinuity in dielectric constant across Si/SiO_2 interfaces has been handled by the method of images.

3 SIMULATION RESULTS

In FinFET, the fin is usually made lightly doped. Even if the fin is undoped, the unavoidable background doping gives rise to at least one ionized dopant being present at a random location within the channel. Also, if an electron becomes trapped in a defect state at the interface or in the silicon body, it will introduce a fixed charge in the channel region. This potential source of localized charge gives rise to localized barrier to current flow. Device behavior is affected by this localized barrier from both electrostatic (effective increase in channel doping) and dynamics (transport) points of view. The effects become dominant for smaller fin width. The size of fin extension on both sides of gate also affects the severity of the effects due to unintentional doping on device performance. Also there exists a strong correlation between reduction in drain current due to unintentional dopant and its position in the channel.

Figure-3 depicts the output characteristics of the FinFET device shown in Figure-1 and Figure- 2. Results obtained using Poisson-EMC (P^3M approach) is in good agreement with that obtained by using FMM-EMC as shown in Figure-3.

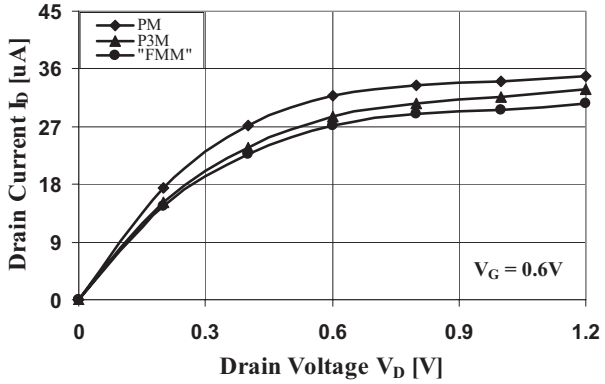

Figure 3: Output characteristics of FinFET devices.

Note that the threshold voltage, as seen in transfer characteristics, Figure-4, is negative due to the use of n^+ polysilicon gate. A nominal threshold voltage of 0.2–0.4 V for n-channel FinFET can be achieved using metal gates with work function close to the mid band-gap of silicon (~4.6eV). Achieving symmetric threshold voltages for both n-channel and p-channel FinFET requires metals with different work functions [12].

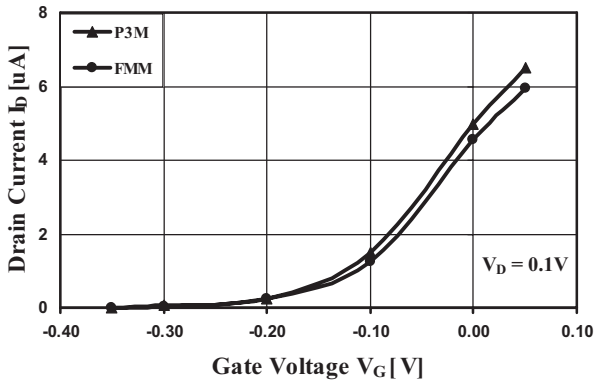

Figure 4: Transfer characteristics of FinFET device.

We have used FinFET device with L_g = 20 nm, S/G gap = D/G gap = 10 nm, Fin thickness = 10 nm, and t_{ox} = 2.5 nm, Source/Drain doping = 2×10^{19} /cm^3 and intrinsic fin.

Drain current varies nonlinearly with fin extension length [13]. It is important to note that reduction in drain current due to increase in S/G gap is more pronounced than that due to increase in D/G gap. This is due to the fact that source side extension length (S/G gap) has more influence on threshold voltage than drain side (D/G gap) does.

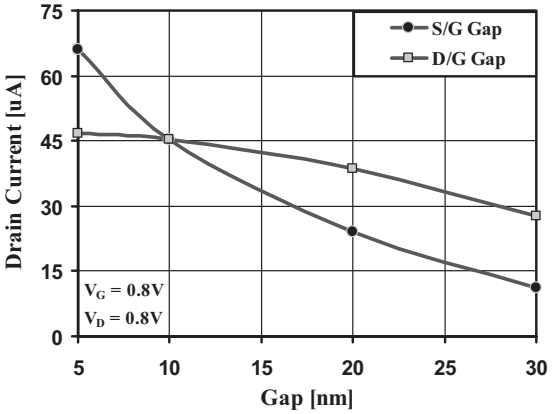

Figure 5: Drain current vs. fin extension length.

Scattering events occurring near the low field source-end of the channel also have larger impact on the drive current. With increase in S/G gap, carriers suffer more scattering on their way to the drain end. High electric field near the drain end forces carrier towards drain contact thereby carriers have less chance of back scattering. With increase in D/G gap therefore the reduction in drain current is less compared to that due to the same amount of increase in S/G gap.

The effect of fin width on drain current reduction due to unintentional dopant has been observed. For increasingly smaller fin width while keeping other parameters constant, the reduction in drain current becomes more pronounced. From simulation results it can be concluded that smaller geometry devices will have more impact on performance due to unintentional single charge in the channel region. Fin thickness of 4 nm has been used in these simulations. The dopant is placed near the source end of the channel close to the top interface.

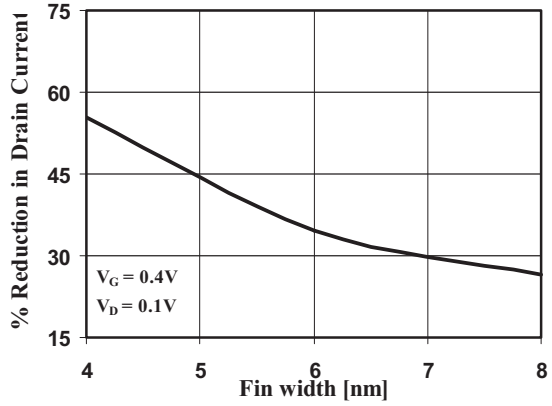

Figure 6: Reduction in drain current vs. fin width.

Fin extension length also affects the decrement in drain current due to unintentional doping. Longer fin extension results in less influence of drain and source fields on barrier created by unintentional dopant and thereby the decrement in drain current becomes more as shown in Figure-7.

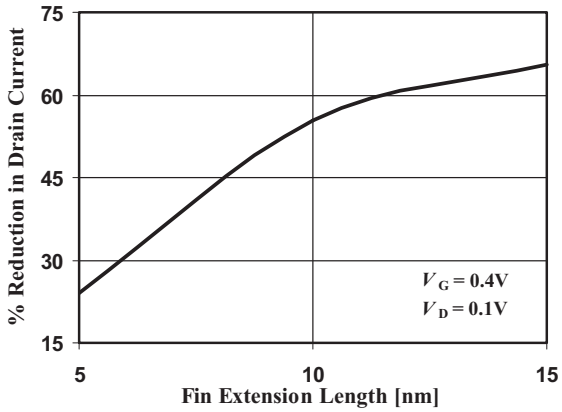

Figure 7: Reduction in drain current due to unintentional doping vs. fin extension length.

Figure-8 shows the reduction in drain current as a function of single ion dopant position along the channel. From the simulation result it is vivid that dopant ion at the source side of the channel affects the drain current most. Near drain end the effect is less pronounced. Also for a particular depth, along the channel from source to drain, the reduction in drain current progressively reduces.

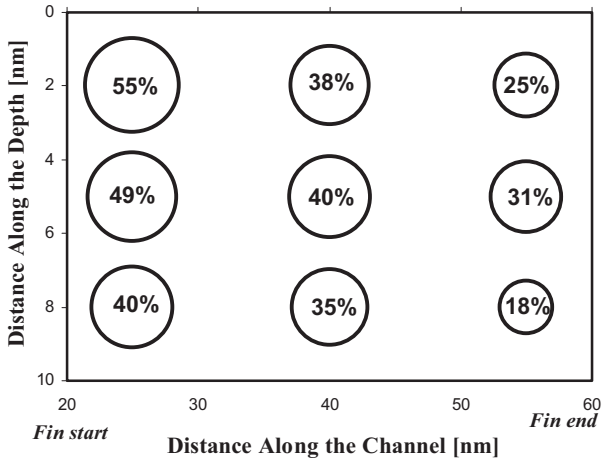

Figure 8: Reduction in drain current vs. position of unintentional dopant along the channel.

For very thin fin, the vertical channels merge towards the center region of the fin. Placing an unintentional dopant at the center region therefore results in largest reduction in drain current as shown in Figure-9. Placing the unintentional dopant close to the interface affects only one channel and therefore the reduction in drain current is less. Fin thickness of 6 nm is used in the simulation.

The effect of unintentional doping becomes dominant near sub-threshold regime where number of mobile carriers in the channel is very low. As gate voltage increases, the electrons in the channel begin to screen the localized potential of the single dopant ion, thus reducing its impact on the current flow as shown in Figure-10.

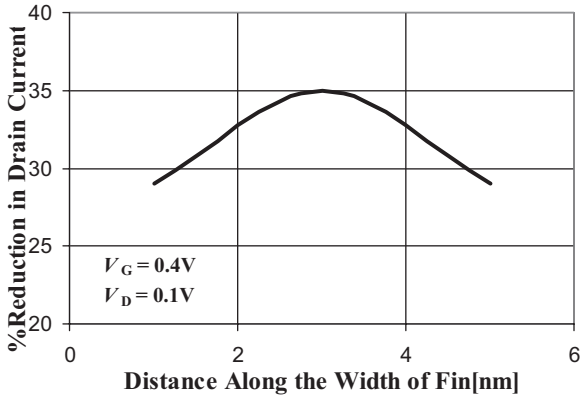

Figure 9: Reduction in drain current vs. dopant position along the width of the fin.

The simulation result is for dopant placed at the center region of the channel close to the top interface.

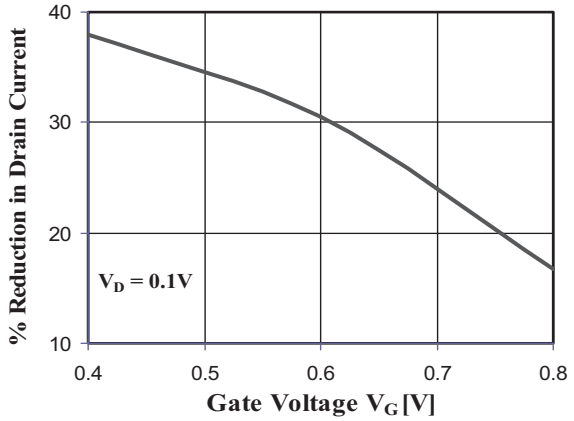

Figure 10: Screening behavior of channel electrons on the reduction of drain current due to unintentional dopant.

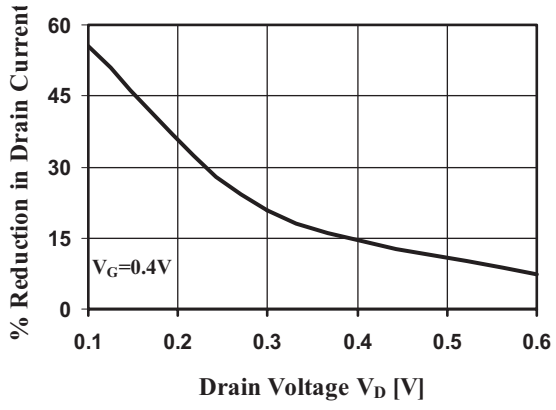

Figure 11: Influence of drain bias on reduction of drain current due to unintentional dopant.

Similarly, an increase in drain voltage results in smaller reduction in drain current due to more acceleration of carriers over the localized barrier produced by unintentional dopant as shown in Figure-11. Dopant is placed near the source end of the channel in the simulation.

4 CONCLUSION

In this work, we have presented the results obtained from 3D Monte Carlo simulation of FinFET devices. Use of FMM algorithm with Monte Carlo simulator speeds up the simulation significantly and the results are comparable with those obtained by P^3M approach. Also effects of unintentional doping on device behavior have been investigated. Presence of unintentional dopant in the channel can significantly alter the device behavior for low drain bias. One has to take into account transistor mismatches due to unintentional doping when performing circuit designs.

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