The Design of a Silicon Wire DRAM Cell for Very Dense DRAM Architectures

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ABSTRACT

A new DRAM cell using silicon wire technology is proposed with the intention of minimizing the cell area. The DRAM cell is composed of a vertical Silicon Wire FET (SWFET) that functions as the pass-gate transistor and a layer of high dielectric constant material that forms the capacitor. In this study, the threshold voltage of SWFET is analyzed as a function of both silicon wire radius and doping density. This analysis consequently leads to determining transistor's maximum current carrying capability and off-current for evaluating the cell read/write speed and refresh time, respectively. Tungsten is used as a gate material because it yields high threshold voltages and produces small off-currents. The long effective channel length eliminates the necessity of forming Lightly Doped Drain (LDD) regions. The cell capacitor is designed to hold the industry-standard 32 fCoul static charge and it is formed from a high dielectric constant material depending on the body radius of the silicon wire.

Keywords: vertical FET, DRAM cell, nano wire, silicon wire, silicon wire transistor.

1 INTRODUCTION

The demand for high density DRAM has been leading the way to build compact memory cells with vertical transistors [1, 2] to further minimize the cell area [3-5]. The thought of using vertical Surrounding Gate Transistors (SGT) [6, 7] in ULSI [8, 9] produced a platform to model 3D DNA structures in silicon [10-12]. Devices composed of silicon and other semiconductor wires [13, 14] may implement complex 3D structures with ease in the next generation IC technology as the sub-0.1 um fabrication complexities increase [15]. Vertical and horizontal silicon nanowire growth has already been investigated using different catalysts and growth techniques [16-18]. Electrical transport characteristics of single-strand silicon nanowires have been extensively studied as a function of body doping density [19].

In this manuscript, we propose a new DRAM cell composed of a vertical Silicon Wire Field-Effect Transistor (SWFET) stacked on top of a high-dielectric constant capacitor that holds the industry-standard 32 fCoul charge.

2 THE DRAM CELL STRUCTURE

The DRAM cell used in the simulations is shown in Figure 1.

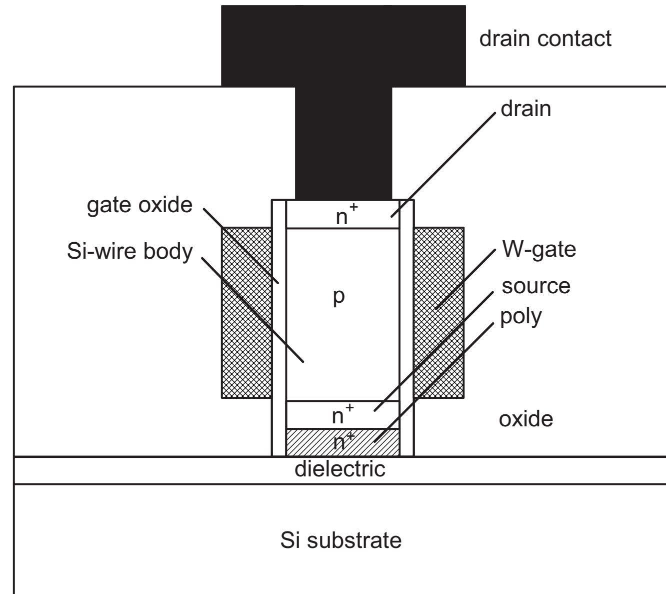

Figure 1: The cross section of the silicon wire DRAM cell used in simulations.

The cell consists of a 5 nm thick, high permittivity dielectric layer and a vertical SWFET that functions as a pass-gate transistor. Tungsten is used as a gate material to form a high threshold voltage for the transistor and produce low off-current. The gate oxide is 5 nm thick native SiO_2. A long effective channel length of 0.8 um limits the maximum electric field to 1.25×10^4 V/cm at the drain for Vds = 1 V. This maximum value is an order of magnitude less than the critical electric field for silicon (2×10^5 V/cm), and it consequently eliminates the necessity of Lightly Doped Drain (LDD) regions. The transistor body is assumed to be uniform by p-type in-situ doping during wire growth. The n^+ source contact has a Gaussian profile and it is assumed to be formed by out-diffusing n-type dopant from an n^+ polysilicon source; the n^+ drain contact has also Gaussian profile and assumed to be formed by n-type ion implantation.

The simulations were carried out using Silvaco's ATLAS 3D device simulation platform.

3 THRESHOLD CHARACTERISTICS OF THE SWFET

To understand the effect of wire body (body effect) on the threshold voltage, V_T, silicon wire radius is changed between 10 and 100 nm and the body doping density between 10^{15} and 10^{18} cm^{-3} as shown in Figure 2. This

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complete analysis on threshold voltage will, in turn, be used to determine the transistor's maximum current drive in terms of its dc transconductance and off-current for evaluating the cell read/write speed and refresh time, respectively.

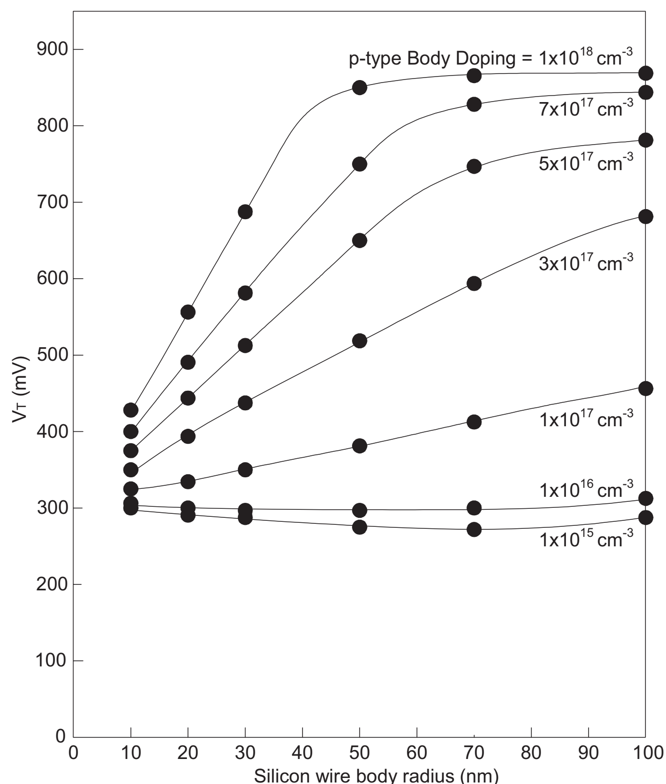

Figure 2: V_T vs. body radius.

In Figure 2, V_T is found relatively unaffected by the radius change if the body doping concentration is kept under 10^{16} cm^{-3}. This is due to the flat-band voltage, V_{FB}, determining the value of V_T rather than the ionized acceptor charge density, Q_A, or the semiconductor surface potential, ψ_S, at the onset of strong inversion as described by a well-known equation in (1).

$$V_T = V_{FB} + \psi_S + \frac{Q_A}{C_{OX}} \tag{1}$$

Note that in (1), Q_A can be written in terms of the ionized acceptor concentration, N_A, and the thickness of the depletion region, x_A, at the onset of strong inversion.

$$Q_A = qN_A x_A \tag{2}$$

As the body doping concentration increases, Q_A becomes the dominant parameter in (1). One observes that V_T increases linearly with the body radius for doping concentrations below $3x10^{17}$ cm^{-3} in Figure 2. This is due to the fact that at these concentration levels, the body radius becomes smaller than x_A and it replaces x_A in (2) for a fully-depleted body. Consequently, a linear increase in body radius increases both Q_A and V_T linearly. This linear relationship, on the other hand, does not hold for doping concentrations in excess of $3x10^{17}$ cm^{-3}. In the extreme case of $N_A=10^{18}$ cm^{-3}, for example, V_T barely changes over 865 mV for a wire radius larger than 50 nm because of a partially-depleted silicon wire body. As will be explained later on, this result determines the lowest cell read/write speed and the highest refresh time in this study.

4 SELECTION OF THE CELL DIELECTRIC

The dielectric layer under the source of SWFET forms the cell capacitor. Since the capacitor is directly under the source of the SWFET, the capacitor area is determined by the area of the source. In order to create the industry-standard 32 fCoul charge in the capacitor, the dielectric material has to be selected from a list of high dielectric constant materials. New advances in dielectrics promise few candidates compatible with silicon. Besides the fundamental material properties such as band gap and high dielectric constant, thermal stability, interface stability and reliability must also be considered in determining a suitable dielectric material.

Figure 3 shows the dielectric constant of the cell capacitor that holds 32 fCoul charge as a function of wire body radius. Note that the thickness of the dielectric is 5 nm and the operating power supply voltage is 1 V for the DRAM cell. For a wire radius of 20 nm and lower, the figure shows that a high dielectric constant material needs to be used for the capacitor. Even though Ti and Ta oxides show dielectric constants in excess of 100, their small band gaps produce substantial gate leakage currents and their interface with silicon create high carrier trap density to limit their usage for FETs [20]. For larger wire radii, such as 50 nm, brings HfO_2 with a dielectric constant of 25 into the picture. Current studies show that this dielectric is mostly compatible with silicon processing up to 700 ^{o}C and reliable as a gate oxide [20, 21]. Using the familiar SiO_xN_y with a dielectric constant of 5.7 [20] as a cell dielectric requires wire radius of only 100 nm.

5 DC TRANSCONDUCTANCE AND READ/WRITE SPEED

The current drive capability of SWFETs is measured in terms of their maximum dc saturation transconductance, gmsat. This quantity is plotted as a function of body doping density in Figure 4 for different values of wire radius. In this figure, gmsat decreases as the body doping concentration is increased; the slope of gmsat becomes steeper as the body radius approaches towards100 nm. This is in general agreement with the results of Figure 2, in which V_T increases with the body doping density. Another observation in Figure 4 is the fact that gmsat stays unchanged until N_A reaches 10^{16} cm^{-3}. This is also

consistent with Figure 2, which states that V_T does not change with the body doping concentration until N_A is greater than 10^{16} cm^{-3}.

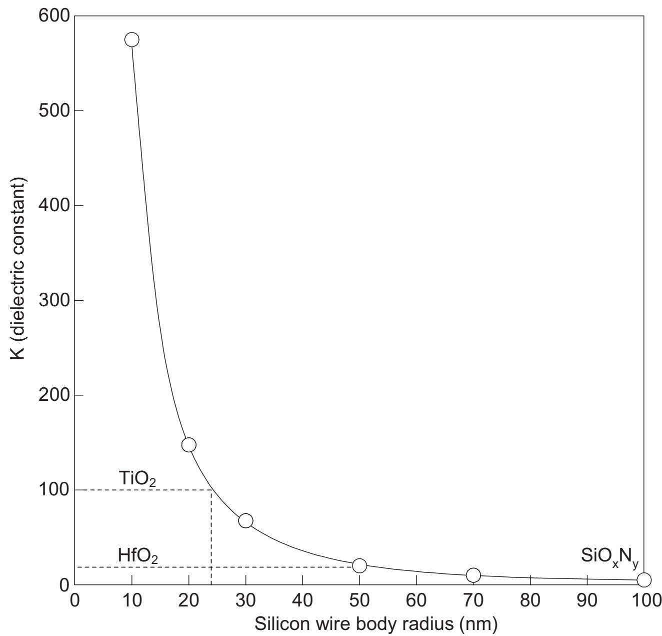

Figure 3: Dielectric constant vs. body radius to hold 32 fCoul charge in the DRAM cell.

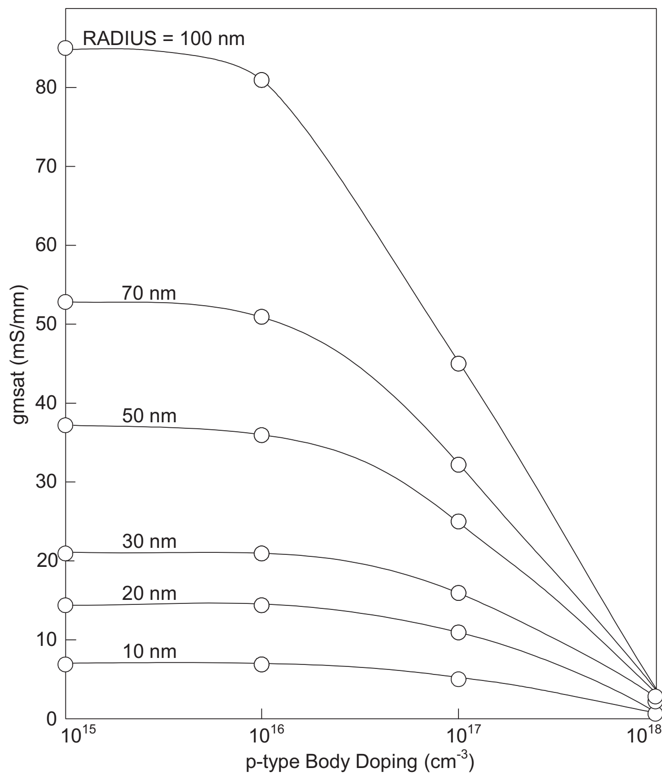

Figure 4: Maximum saturation dc transconductance (gmsat) vs. body doping concentration.

The read/write speed, T_S, is a direct consequence of the Gauss law and inversely proportional to gmsat as shown in (3):

$$T_S \alpha \frac{C_{cell}}{gmsat} \tag{3}$$

Where, C_{cell} is the value of the cell capacitance.

The simulation results of T_S as a function of body doping are shown in Figure 5 for different values of body radius. In this figure, T_S stays relatively unchanged with increasing values of N_A and its value increases with decreasing values of body radius until $N_A=10^{17}$ cm^{-3}. Beyond $N_A=10^{17}$ cm^{-3}, however, the value of T_S drastically increases with body doping density; the rate of this increase is higher as the wire radius increases. Both of these observations are consistent with the way the dc transconductance changes in Figure 4 and (3).

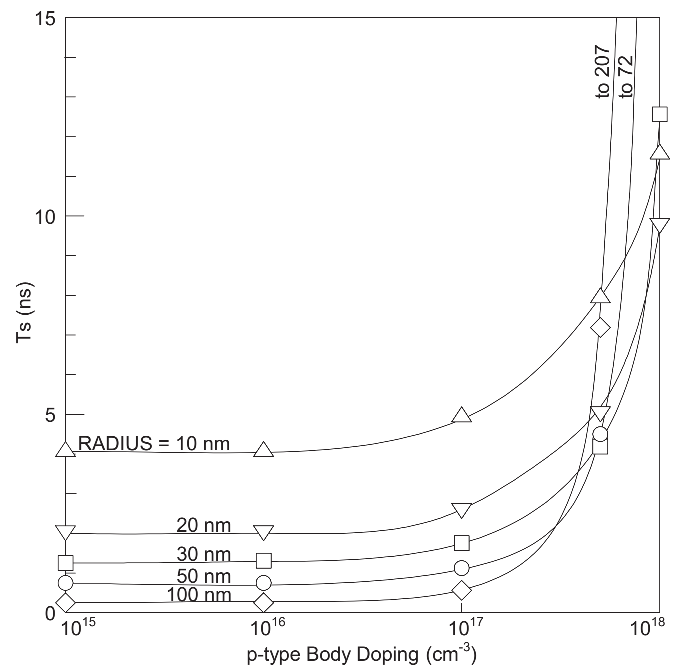

Figure 5: Read/write speed (Ts) vs. body doping concentration.

6 OFF-CURRENT CHARACTERISTICS

An element of importance in determining the proper SWFET for the cell is the magnitude of the off-current, I_{OFF}, since it is inversely proportional to the cell refresh time, T_R as described in (4). In this equation, Q_{cell} is equal to 32 fCoul when the DRAM cell is charged to V_{DD} = 1 V.

$$Q_{cell} = I_{OFF} T_R \tag{4}$$

Figure 6 illustrates how I_{OFF} changes with N_A at a fixed body radius of 50 nm. The change in I_{OFF} is a direct consequence of the change in V_T, i.e. larger values of V_T

results in smaller values of I_{OFF}. One would anticipate that the maximum I_{OFF} value increases beyond 10^{-11} A in Figure 6 as the wire radius becomes smaller than 50 nm. This is because of the range of V_T values in Figure 2 monotonously decrease as the wire radius is reduced.

Figure 6 also illustrates the change in T_R as a function of body doping concentration for the 50 nm radius wire; the T_R values are directly calculated from (4) for Q_{cell} = 32 fCoul.

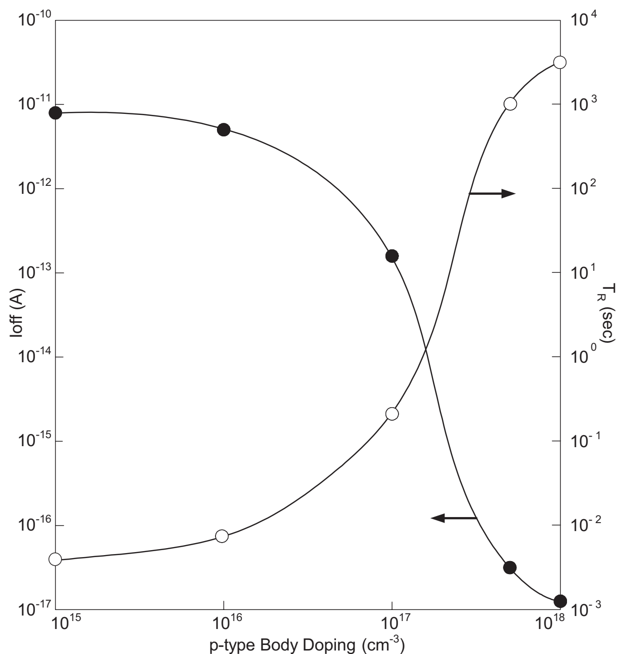

Figure 6: The off-current, I_{OFF}, and refresh time, T_R, as a function of body doping concentration for a fixed 50 nm body radius.

7 CONCLUSIONS

A new DRAM cell is proposed using a vertical SWFET as a pass-gate transistor in series with a high dielectric constant material such as HfO_2 that forms the cell capacitor.

Throughout the device simulations, the body doping concentration and radius are changed between 10^{15} and 10^{18} cm^{-3} and 10 and 100 nm, respectively. The effective channel length of the SWFET was kept at 0.8 um to avoid impact ionization; dielectric and native gate oxide thicknesses were kept at 5 nm, and the power supply voltage was 1 V.

First, the characteristics of the SWFET are obtained in terms of its threshold voltage, maximum saturation dc transconductance, and off-current as a function of both wire body radius and doping concentration. Second, a suitable high dielectric constant material is selected for the cell capacitor to hold the industry-standard charge of 32 fCoul. Third, the read/write speed and refresh time for the DRAM cell are analyzed as a function of SWFET and the capacitor characteristics. This study revealed that the proposed DRAM structure is a good candidate for implementing the next generation of dense DRAM architectures with cell performance and characteristics comparable to those reported in the literature.

Further studies will include using Silvaco's ATHENA process simulator in conjunction with ATLAS device simulator for more accurate device characteristics.

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