Using ultra-long nanotubes to make identical CNT FETs

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ABSTRACT

We have fabricated a CNTFET with S-D spacing of 25 μm on a nanotube that was originally over 360 μm in length. By repeating this process, it should be possible to fabricate many CNTFETs on the same nanotube with identical characteristics. This takes an important step towards a fabrication technology suitable for the manufacture of *integrated circuits* based on CNTFETs.

Keywords: nanotube, array

1 INTRODUCTION

Carbon nanotubes have attracted attention in recent years due to their excellent electrical, mechanical and chemical properties potentially useful for a variety of applications[1]. Single-walled carbon nanotubes (SWNTs) show one-dimensional (1D) molecular phenomena ideally suited for building miniaturized devices such as transistors.

We recently demonstrated that cm scale 1d arrays of single walled carbon nanotubes can be grown which are electrically continuous along their entire length[2, 3]. These tubes have an extraordinary aspect ration. Additionally, we demonstrated that these macroscopically long nanotubes have conductivity better than copper. This opens the door to using nanotubes as interconnects in integrated and even discrete circuits with macroscopic dimensions.

One potential advantage to these ultra-long nanotubes is that they can be used to make many CNTFETs with identical electrical properties. This is possible because the nanotube is so long, many different CNTFETs can be fabricated out of one nanotube. This would be a step in the direction of fabricating large scale integrated circuits out of carbon nanotubes, which will eventually require strict tolerance on device-to-device variation. By using *one* (long) nanotube to make many devices, device-to-device variation could be reduced or eliminated. Using our 4 mm long nanotubes, with S/D electrodes spaced every 4 μm, it could be possible to fabricated 1000 nanotubes transistors with identical electrical properties.

In this conference paper, we describe a carbon nanotube field effect transistor (CNTFET) fabricated from a mm scale nanotube that has a source-drain spacing of 25 microns. The CNTFET depletion curve and I-V curves are presented. This clearly shows that it is possible to make short CNTFETs out of long nanotubes.

2 SYNTHESIS AND FABRICATION

2.1 Synthesis

The synthesis processes are described in detail[2, 3]. Briefly, we started with a 4-inch Si wafer with a precoated 500 nm thick SiO_2 film as the substrate. After wafer cleaning, a thin Cr adhesion layer (50 nm) was deposited by e-beam deposition, followed by 200 nm gold films. 0.8 μm positive photoresist (Shipley 1808) was spun on the substrate and then patterned by photolithography to form the gold control layer. Nanoparticle catalyst was prepared by adding 0.3 g of alumina nanoparticles (Degussa), 0.05 mmol of $Fe(NO_3)_3 \cdot 9H_2O$ (Aldrich), and 0.015 mmol of $MoO_2(acac)_2$ (Aldrich) to 300 ml DI water (18 MΩ.cm). The mixture was stirred for 24 hours and sequentially sonicated for 1 hour. Then the suspension was dropped onto the pattern and dried at room temperature. By lift-off of the photoresist in acetone, patterned catalyst is left on the substrate.

CVD[4] was carried out using a 3” Lindberg furnace. A gas recipe that favors the synthesis of ultra-long and high quality SWNTs was adopted in the experiment. After heating the 3” quartz tube to 900°C under an argon atmosphere, the argon was replaced by a co-flow of 1000 sccm methane (99.999%), and 200 sccm hydrogen for 15 minutes. All the processes were performed under manual control, including purging Ar, increasing the temperature, flowing active gases and cooling down the system in the Ar atmosphere after growth process finished. After growth, the nanotubes were imaged by SEM (S-4700-2 FESEM, Hitachi, Japan). Fig. 1 shows an SEM image of the nanotube used in this study before electrode deposition.

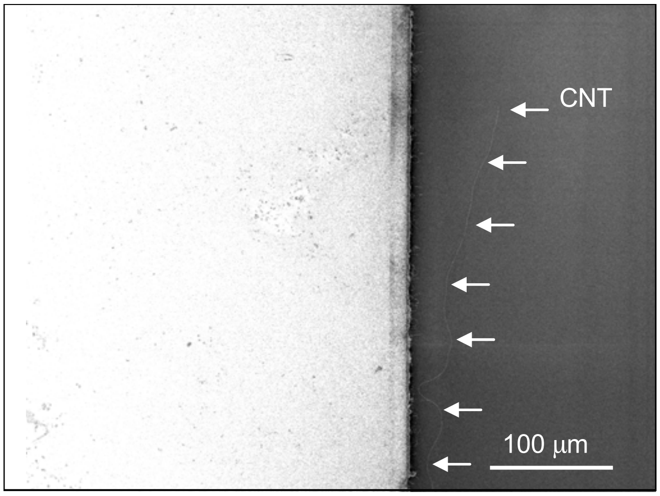

Fig. 1: SEM image of nanotube after growth. This nanotube was 360 μm long.

2.1 Electrode fabrication

After synthesis, electrodes were patterned using electron-beam lithography and liftoff via e-beam evaporation. For the metallization layer, a bilayer of 5 nm Ti/100 nm Au was used. No post-metallization anneal was performed. Fig. 2 shows an SEM image of the nanotube transistor after the metallization was applied

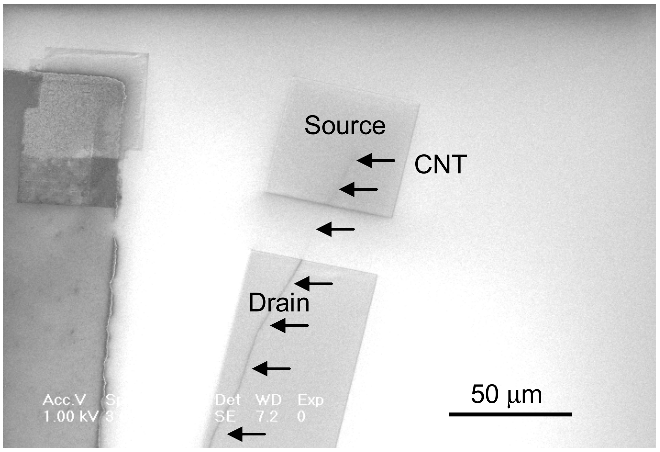

Fig. 2: SEM image of nanotube transistor after electrode (source/drain) deposition.

3 ELECTRICAL PROPERTIES

3.1 Depletion Curve

In Fig. 3, we plot the low-bias depletion curve measured at room temperature in air. (The substrate was used as the back-gate.) The depletion curve shows p-type behavior, consistent with prior published data on CNTFETS[1]. Hysteresis is also observed, due possibly to trapped charges in the oxide. This is also observed in our shorter nanotubes, and so is not unique to our cm scale CNTs. The on-off ratio is greater than 100.

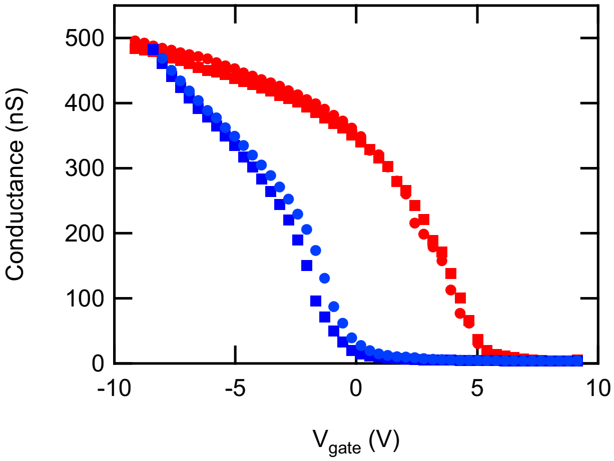

Fig. 3: Depletion curve measured at room temperature in air.

3.2 I-V curve

In Fig. 4, we plot the measured source-drain I-V curve at various substrate (gate) voltages. Transistor action is clearly visible, as well as clear saturation in the source-drain current at high source-drain bias voltages.

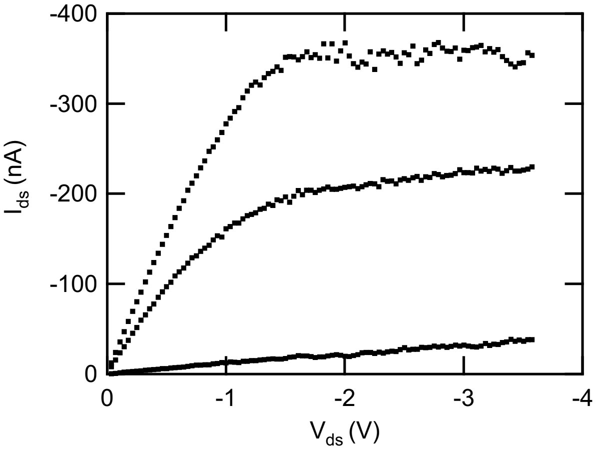

Fig. 4: Measured I-V curves at various gate voltages from 0 to -6 V at room temperature in air.

4 DISCUSSION

Recently the issue of the mechanism of transistor action in nanotube transistors has been discussed by several groups. Heinze[5] has presented arguments that the sole effect of a gate is to modulate the Schottky-barrier contact resistance, not the bulk resistance, implying that a carbon nanotube transistor is a Schottky barrier device. However, these arguments generally considered short (micron length) carbon nanotubes. Javey[6] has recently developed contact technology to significantly suppress the Schottky barrier contact resistance.

Because we have intermediate length CNTFETs in this conference paper, our data may provide some useful insight into this discussion. In particular, our CNTFETs are definitely in the diffusive limit. In our prior work on ultra-long nanotubes[3], we showed that the mean-free path is about 1 μm; this is much shorter than the 25 μm source-drain spacing presented in this paper. This is an intermediate length, where the effect of the gate on the contacts and the channel resistance may be comparable. Future studies of the behavior of CNTFETs as a function of S-D spacing could be performed on the *same* nanotube by fabricating many CNTFETs with different source-drain spacing on one tube.

5 CONCLUSION

We have fabricated a CNTFET with S-D spacing of 25 μm on a nanotube that was originally over 360 μm in length. By repeating this process, it should be possible to fabricate many CNTFETs on the same nanotube with identical characteristics. This takes an important step towards a fabrication technology suitable for the manufacture of *integrated circuits* based on CNTFETs.

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