Fabrication and characterization of MOS transistor tip integrated micro cantilever

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ABSTRACT

We fabricate and characterize the metal-oxide-semiconductor (MOS) transistor tip integrated micro cantilever, which is proposed for a future high-density data storage system. The integrated MOS transistor tip as the sensing part has some advantages; it detects the electric signal with the fast speed compared with the previous SPM probes, and it can reduce the required equipments such as the lock-in-amplifier. The MOS transistor tip is fabricated 3-dimensionally, utilizing the lateral diffusion and the anisotropic wet etching with TMAH solution, since the etch rate of {211} plane is much higher than those of {100} or {111} planes. The gate area is formed by self-aligned technique, using crystallographic dependant wet etching. The well-known convex corner compensation pattern is used for the gate length control during the tip fabrication process. The characteristics of the fabricated device are measured and the results show the well-established detection properties.

Keywords: metal-oxide-semiconductor (MOS) transistor tip, future high-density data storage system, self-aligned technique, crystallographic dependant wet etching, convex corner compensation

1 INTRODUCTION

The MOS transistor is one of the most important devices in the nano-technology and nano-science era. From the first invention in 1960, it has been applied to the many electronic devices such as CPU, memory and so on, and nowadays, remarkably expands to other application fields [1]. The MOS transistor has several advantages in the production cost, the power consumption and the integration with other circuits of the device [1-2]. Especially, because of the usage of the common semiconductor technologies, it is easily integrated with the amplification and signal processing units and thus reduces the production costs. Moreover, its current output changes with the gate condition, and it is sensitive to the external signal. Since the sensitivity is related to the power consumption, the high sensitivity means the low power consumption. The low power consumption and the high sensitivity become more important as the device size goes down, and from these points of view, the MOS transistor is the most promising unit of the nano-scale devices.

Those advantages make the MOS transistor as a main component of the micro and nano sensors as well as the circuit unit. The representative sensor using the MOS transistor is the ISFET (Ion Sensitive Field Effect Transistor) which is used for the pH sensor [3-5]. The ISFET is almost same structure as the MOS transistor, and senses the pH states detecting the ion change at the gate in the liquid. The other application devices of the MOS transistor such as the charge sensor [6], the pressure sensor [7] and the gas sensor [8] have the almost same detection mechanism. Since the gate channel is sensitive to the external signal, the MOS transistor can be the suitable solution for sensing these external signals. However, in contrast to the merits on the fabrication process, the MOS transistor with plane shape has some limitation when the device detects the local points on the surface. The MOS transistor with the tip shape is required to solve the limitation on the local point detection. The sensor with the tip shaped MOS transistor is reported [9], but it has some problems in fabrication such as the misalignment.

The most SPMs detects the signal at the tip end, and the operation speed is related to the mechanical resonance frequency of the cantilever. Generally, it is not high enough, and the array is introduced to overcome the low operation speed [10-11]. However, with the array structure, the fabrication requirement such as the uniformity becomes more tight, which can be one of major obstacles for the

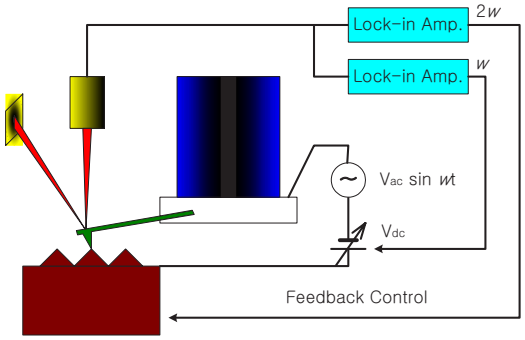
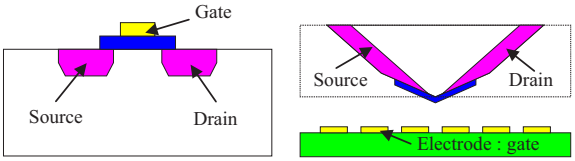


Figure 1: Schematic view of the commercial SPM system (EFM)



(a) Common MOS transistor (b) Proposed MOS transistor

Figure 2: Comparison of the proposed MOS transistor tip with common MOS transistor

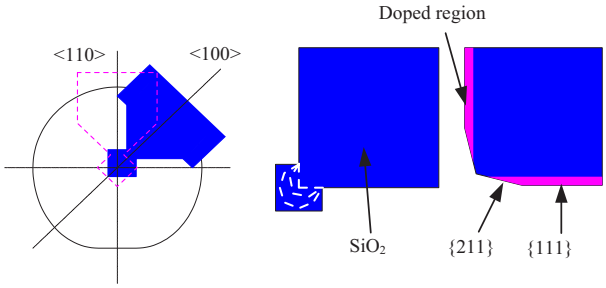
commercialization of the devices. Especially, since the scratch detection of the micro devices requires the high speed, the low operation speed of the cantilever must be solved. The MOS transistor as the sensing part of the SPMs can be the solution, since the MOS transistor has high operation speed, which is not determined by the mechanical resonance. Moreover, MOS transistor at the tip end reduces the additional equipments such as lock-in-amplifier in one of the SPMs, EFM (Electrostatic Force Microscope) system as shown in Figure 1 [12]. The additional equipments make the entire system large, so it becomes another obstacle.

In this paper, we fabricated and characterized the 3-D MOS transistor integrated micro cantilever (Figure 2), which has some advantages on the gate length control and the easy fabrication. The MOS transistor as the sensing unit has high sensitivity and the high operation speed, and they show the prospective to overcome the limitation. Moreover, it has simple fabrication process with wet etching, and the length of the gate channel can be easily controlled. The device can detect the local area, and also can be applied to the micro-topology sensor, ion sensor, and the probe head for high-density data storage system.

2 DESIGN

There are many methods to make a tip. In addition to the well-known isotropic dry etching method [9-11] and bulk etching/deposition method [13], special methods such as a rocket tip method [14], an INCISIVE tip method [15] and a deep trench refilling method [16] have been proposed and researched. The reason to require the tip is to place it properly on the desired small area, and to make the better sensitivity about the external signal. However, it's not easy to make the MOS transistor in those tips, since they have out-of-plane structures in most cases. Although the tip with MOS transistor is reported, some problems such as the misalignment may happen in the fabrication process [9]. In this paper, we use the in-plane tip to easily integrate the MOS transistor with the special etching techniques [17].

Figure 3 shows the design of the 3-D MOS transistor tip fabrication. The cantilever is fabricated with distinct alignment technique in the conventional wet etching as shown in Figure 3 (a). In usual micro-fabrications, the cantilever body is parallel to the <110> direction. In this paper, the cantilever body is parallel to the <100> direction and the tip is parallel to <110> direction for the self-alignment of the MOS transistor channel. The designed



(a) MOS tip alignment (b) tip fabrication process

Figure 3: Process design of the MOS transistor tip integrated cantilever

process is shown in Figure 3 (b). First, tip patterning is performed and the convex corner compensator is used for the sharp tip formation. After the tip formation with the anisotrophic wet etching, the boron doping process for the drain and the source parts is followed. The upper oxide layer protects the upper side doping, and the only lateral diffusion is performed. In this case, since all sides of the cantilever are doped, the tip area must be removed for the gate part. The crystallographic dependant wet etching is carried out to make the gate channel after the oxide layer is removed. This is the self-aligned technique, since the etch rate of the {211} plane of Si wafer is much faster than those of the {100} or {111} planes [18], and the channel of the gate part is automatically formed. After another floating part of the oxide layer is removed, the MOS tip on the cantilever is fabricated with the re-growing of the gate oxide layer.

3 FABRICATION

Figure 4 shows the detailed fabrication process. Fabrication starts with a 10μm N-type (100) epitaxial layer covered with a 0.7μm-thick thermal oxide layer on 500μm thick P-type (100)-oriented Si wafer. After the oxide layer is patterned, first boron doping is performed for the electrical connection. This boron doping requires the high concentration, as the doped area must have high electrical conductivity. The whole oxide layer is removed and another 1.5μm-thick thermal oxide layer is re-grown. This layer requires high thickness, since it is used for both the etching and the doping mask. After the cantilever structure is patterned, the anisotrophic wet etching is performed for 200 min with 50oC TMAH solution. With the application of the convex corner compensator, the sharp tip can be obtained at the end of the cantilever. After the removing the floating oxide layer, the boron is laterally diffused for the formation of the source and the drain of the MOS transistor tip. During the diffusion process, the thin oxide layer is grown on the tip area. Since this layer is thinner than the upper oxide layer, only the oxide layer on the tip area is removed, whereas the upper oxide layer remains due to the thickness difference. The convex corner is etched away using another 30min anisotropic etching with 50°C TMAH solution. Fast

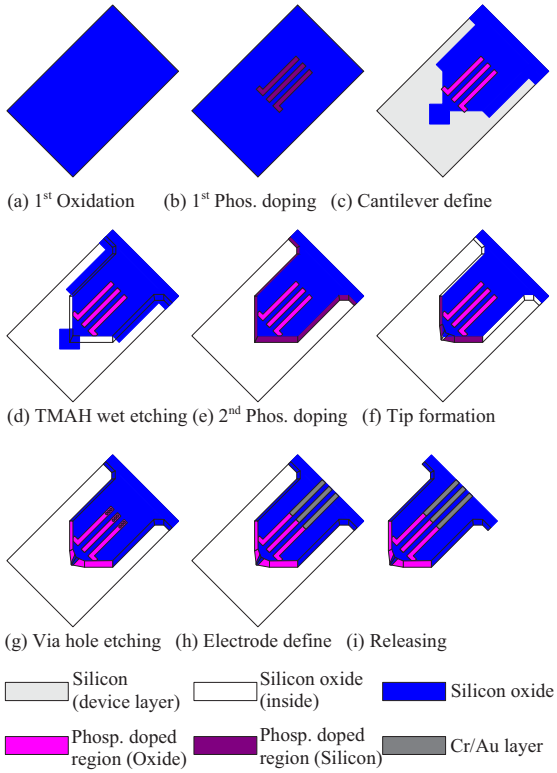


Figure 4: Fabrication process

etching of {211} planes makes the gate area in the convex corner, and electrically separates the source and the drain areas. The floating oxide layer is removed and a 50nm thick gate oxide layer is re-grown using a dry oxidation. For the electrical connection, the via hole patterning is performed and Al deposition/patterning is followed. To protect the device layer from the undesired TMAH wet etching during the releasing process, it is painted with the black wax and the glass wafer is bonded to prevent the direct contact between the wax and TMAH solution. The fabrication process is finished with the removal of the black wax.

The gate area formation of the MOS transistor tip is the most critical part of the process. The etch rate difference between the Si crystal planes automatically makes the gate area, since the etch rate of the {211} plane of Si wafer is much faster than those of the {100} or {111} planes. It does not require the additional aligning process, the so-called self-aligned technique.

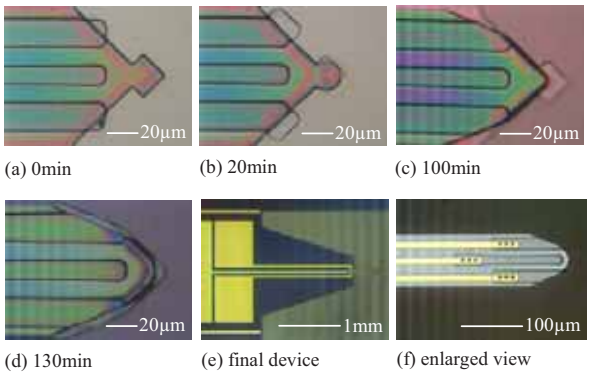


Figure 5: Tip formation process in sequence (TMAH 50°C)

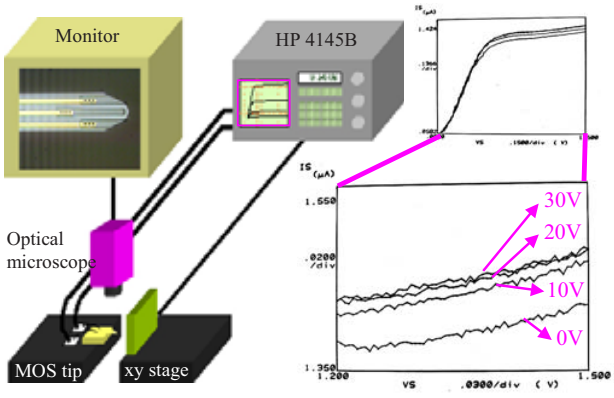
4 RESULT AND DISCUSSION

4.1 Fabrication result

The integrated MOS transistor tip is the most important part of the device as a sensing part. Figure 5 shows the tip fabrication process with respect to time. Figures from (a) to (d) show the tip patterns with time sequence, which are the initial tip pattern with the convex corner compensator, the tip etching pattern after 20min, the tip pattern with a right angle, and the tip with the gate channel, respectively. As shown in Figure 5 (d), the {211} planes of the corner form the tip channel, since it is quick to etch compared with the {111} planes. Figure 5 (e) and (f) show the fabricated device, which has a 400μm-long cantilever and a 1.5mm-long supporting plate. Since the long supporting plate makes the device flexible, it can be also used to measure the topology of a surface.

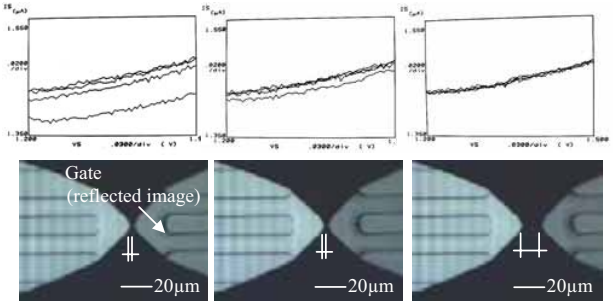
4.2 Characterization of MOS tip integrated micro cantilever

Figure 6 shows the experimental results of the MOS tip integrated cantilever. The probe station and the HP 4145B are used to detect the electrical properties of the device, and the optical microscope is used for the measurement of the distance between the device and the gate plate as shown in Figure 6 (a). The top and the bottom graphs in Figure 6 (b) show the electrical behavior of the fabricated MOS transistor tip, and the variation of the source current with the gate voltage, respectivley. Since the source current is very sensitive to the gate distance, the current variation is rapidly reduced when the gate slightly goes away from the device as shown in Figure 7.



(a) Experimental setup (b) Measured device characteristics

Figure 6: Characterization of the MOS tip integrate cantilever



(a) Contact case (b) Almost Contact case (c) Noncontact case

Figure 7: Electrical behavior with respect to the gate distance

5 CONCLUSION

In this paper, 3-D MOS transistor tip integrated micro cantilever is fabricated and investigated. The 3-D shape is obtained using a crystallographic dependant wet etching and convex corner compensator, and the MOS structure is generated using the lateral boron doping and self-aligned technique with crystallographic dependant wet etching. The characteristics of the device are investigated, and the measured data show well-established properties, which present the promising aspect for the micro-scale topology sensor, the charge sensor, and SPM probe with the high speed.

For the resolution improvement of surface property inspection, the smaller tip is favored, and the minimization process such as the electrochemical etching is in progress. For the active probe application, the actuator integrated cantilever with the MOS transistor tip is also an ongoing project.

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