Influence of Si nanocrystal distribution on electrical characteristics of MOS structures

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ABSTRACT

In this study, metal-oxide-semiconductor (MOS) structures with Si nanocrystals (nc-Si) embedded in the gate oxide were prepared. It is found that charge trapping in nc-Si with different distributions in the oxide results in distinguished behaviors in MOS electrical characteristics. For the case that nc-Si are confined in a layer, MOS capacitance-voltage characteristics show a flat-band voltage shift with charge trapping, while for the case that nc-Si were distributed throughout the oxide with a high concentration, charging/discharging leads to MOS capacitance magnitude modulation.

Keywords: charge trapping, Si nanocrystal, capacitance modulation.

1 INTRODUCTION

Si nanocrystals (nc-Si) embedded in gate oxide of MOS structures have been studied extensively due to their charge trapping and single-electron charging effect [1-3]. One of the applications of nc-Si is nonvolatile memory device; nc-Si is normally confined in a narrow layer in the gate dielectric near the substrate [1-3]. Charging /discharging in nc-Si leads to the flat-band voltage shifts in MOS capacitance-voltage (C-V) characteristics. However, there are few studies so far on the electrical characteristics of MOS structures with different Si nanocrystal distributions in the gate oxide. In this work, Si nanocrystals with different distributions were embedded in the gate oxide by ion implantation technique. C-V and time-domain capacitance measurements were conducted to study the electrical characteristics of MOS structures. Indeed, it is observed that charge trapping in nc-Si with different distributions in the gate oxide leads to different behaviors in MOS electrical characteristics.

2 EXPERIMENTAL

In fabrication of the MOS structures with different nc-Si distributions in the oxide, first a 30 nm SiO2 films was thermally grown on p-type (100) Si wafers in dry oxygen at 950°C. The Si^+ ions were implanted to the SiO2 films at 1keV, 2keV or 14keV. For the 1kev and 2keV implantations, the dose is chosen to 8×10^{16} cm^{-2}, while for the 14keV implantation, the dose is 3×10^{16} cm^{-2}. Thermal annealing was carried out at 1000°C in N2 ambient for 1 h to induce nc-Si formation. The oxide layer for 14keV implanted sample was thinned at a rate of 10 nm/min in a HF solution of concentration of 50:1. About 17 nm SiO_2 layer was removed such that a high concentration of nc-Si was embedded throughout the gate oxide. For all samples, a 20 nm aluminum layer was then deposited to form gate electrodes. The wafer backside was coated with a layer of aluminum with the thickness of about 1 μm after removing the backside oxide. Finally, metal alloying process was conducted at 425° C in N_2 atmosphere to form ohmic contacts. The 1keV and 2keV implanted samples are used to study the charge trapping in nc-Si confined in a layer but at different depths in the oxide. The 14keV implanted sample is prepared for the study of the charge trapping in nc-Si that are distribute throughout the oxide. The experiment of charging/discharging the nc-Si by applying a constant voltage to the MOS structures was performed with a Keithley 4200 semiconductor characterization system, and C-V and capacitance–time (C-T) measurements were carried out with a HP4284A LCR meter at the frequency of 1MHz.

3 RESULT AND DISCUSSION

Figure 1 shows the C-V characteristics of a MOS structure with nanocrystals confined in a narrow layer in the gate oxide after a negative voltage (–4V) was applied to the gate for 10 sec. Charge trapping in nc-Si in this case leads to a flat-band voltage shift of about 0.7 V. As can be

seen in Fig. 1, the flat-band voltage shift is along the X-axis to the positive voltage, which implies that electron trapping occurs from the gate into the film.

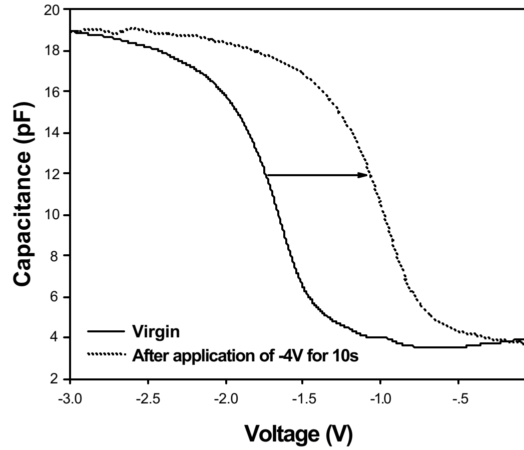

Figure 1: C-V characteristics of a MOS structure with nanocrystals confined in a narrow region in the gate oxide.

Fig. 2 shows the C-V characteristics of a MOS structure with nanocrystals distributing throughout the gate oxide obtained by sweeping the voltage from -3 to 1 V for the following situations: (*i*) virgin; (*ii*) after the first application of +3 V for 160s; and (*iii*) after the second application of +3 V for 60s. As can be seen in Fig.2, the application of +3 V for 160s reduces the capacitance to a very low level (around 600 fF) that is close to the limit of our C-V measurement system. The reduction in the capacitance is due to the charging up in the nc-Si. The application of +3 V for 160s leads to the charging up of most of the nc-Si. The charged nc-Si does not respond to the small AC signal (15mV) as the Coulomb energy is ~ 90 mV for a nc-Si with a size of 4nm in this study. Therefore, the capacitance of the nc-Si decreases, and thus the total MOS capacitance is reduced. On the other hand, the trapped charge in the nc-Si is released by the second application of +3 V for 60s, leading to the recovery of the capacitance, as shown in Fig. 2. Actually, as can be seen in the figure, the second application of +3V for 60s leads to a capacitance ever larger than that of the virgin case. This means that there is some charge trapping in the nc-Si prior to the first application of +3V and the trapped charge can be also released during the second application of the voltage. In this case, charge trapping in nc-Si distributing throughout the gate oxide results in a magnitude modulation in MOS capacitance. Therefore, it is obvious that different nc-Si distributions lead to very different electrical characteristics.

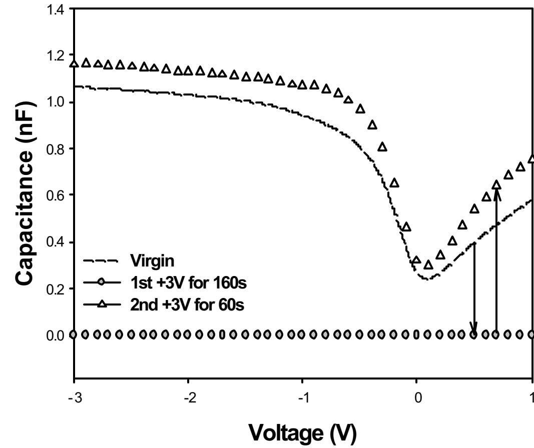

Figure 2: Changes in the MOS capacitance after two applications of +3 V for different durations.

In the first case of nc-Si confined in a narrow layer in the oxide, even a small difference in the location of the peak concentration of nc-Si, which can be realized by varying the Si^+ implantation energy, can yield a significant difference in the memory programming characteristics, as shown in Fig.3 and Fig.4. The flat-band voltage shift ($?V_{FB}$) as a function of the gate voltage (Vg) is shown in Fig.3. Si ions were implanted into 30-nm oxide at 1keV and 2keV, resulting in different nc-Si distributions in the gate oxides. No $?V_{FB}$ appears in the C-V curves at a negative gate bias lower than –1V. As can be seen in this figure, for 1keV and 2keV samples, a higher gate voltage leads to more electrons trapping in nc-Si, and thus a larger $?V_{FB}$. The 2keV-implanted sample shows a larger $?V_{FB}$ at the same Vg than that of the 1keV-implanted sample. This can be attributed to the distribution of the nc-Si. The 2keV implantation leads to a deeper distribution of nc-Si near to the middle of oxide, and thus charge trapping in these devices are more effective to shift the flat-band voltage.

The programming characteristics for different implantation energies are shown in Fig.3. The programming is performed with a negative 15V on the gate for various durations. For the 2keV-implanted samples, programming is possible even less than 1 ms duration, while programming is only applicable more than 1s for 1keV-implanted samples. The difference between

the two types of samples highlights the nc-Si distribution for memory device performance.

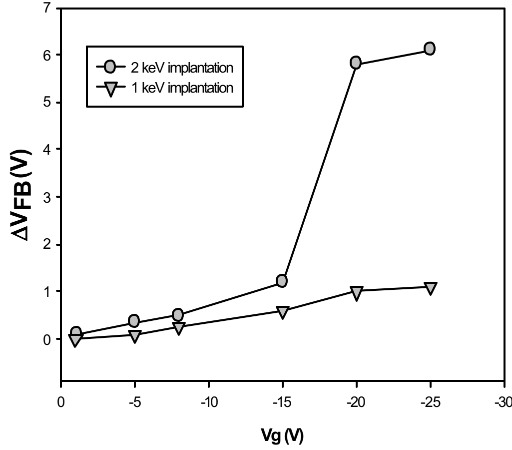

Figure 3: Flat-band voltage shift (?V_{FB}) as a function of the gate voltage. Each negative voltage was applied to the gate for 1 sec.

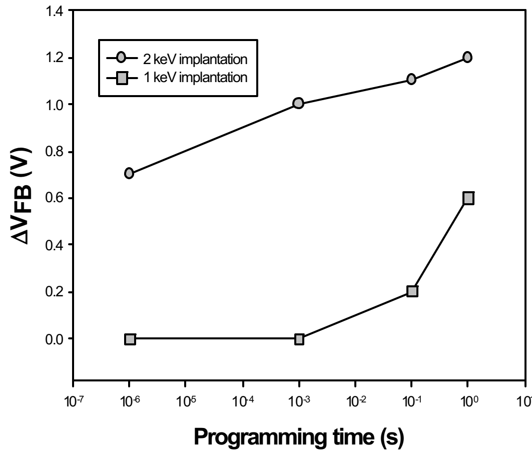

Figure 4: Programming characteristics of devices with different nc-Si distributions. The voltage applied to the gate is -15 V.

Fig. 5 shows the time-domain capacitance characteristic measured at 3V. As can be seen in this figure, the MOS structures with nc-Si distributing throughout the gate oxide shows a capacitance modulation, which is very different from the first case. Such a C-T measurement is carried out at + 3 V. After about 180s, the MOS capacitance was reduced dramatically from the initial value of ~ 0.7 nF to ~ 0.2 nF. In other words, the electrical state of the MOS device was switched from a high-capacitance state (State 1) to a low-capacitance state (State 2). As discussed early, the low capacitance corresponds to a charged state of the nc-Si, while the high capacitance corresponds to a discharged state of the nc-Si. Therefore, State 1 represents the discharged state and State 2 represents the charged state. State 2 can be maintained for ~ 140s. Then the MOS device was switched to State 3 with a capacitance of ~ 1.1nF, which is much larger than that of State 2 and also higher than that of State 1. This indicates that not only the trapped charges associated with State 2 but also some charges that trapped prior to the State 1 have been released. Thus a over-recovery of MOS capacitance can be achieved. If the time scale is extended, switching between different states, which is a random event, can be observed continuously.

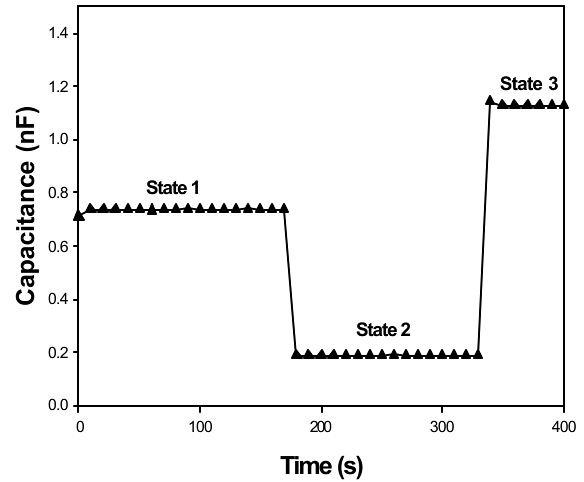

Figure 5: Capacitance modulations in C-T measurement at a constant voltage +3 V.

The observation of the modulation in MOS capacitance can be explained in the following. Charge could be stored in the three elements of the MOS structures, i.e., the nanocrystals, the remaining gate oxide capacitor and the Si depletion layer. The corresponding capacitances of the elements are denoted by C_{nc}, C'_{ox} and C_D, respectively. As illustrated in Fig. 5, the total capacitance C of the MOS structure is

$$C = \frac{(C_{nc} + C'_{ox})C_D}{(C_{nc} + C'_{ox}) + C_D} \quad (1)$$

As C_D is very large under accumulation at - 3V, the total capacitance is approximately equal to

(C_{nc} + C'_{ox}). Due to the existence of a high concentration of nc-Si in the gate oxide, the remaining gate oxide capacitance C'_{ox} is much smaller than the conventional gate oxide capacitance (C_{ox}) without the nc-Si (C'_{ox} is found to be less than ~ 700 fF). Furthermore, as there is a high concentration of Si nanocrystals distributing throughout the gate oxide, the nanocrystals easily respond to the small AC signal in the capacitance measurement if they are uncharged or neutral (i.e., no charges trapped in them). The virgin C_{nc} (i.e., the nc-Si capacitance before charge trapping) should be very large due to the existence of a high concentration of nc-Si. Therefore, the MOS capacitance (C) is approximately equal to C_{nc}, and it will be very large when most of the nc-Si is uncharged. Obviously, the capacitance reduction can be explained in terms of the charge trapping in the nc-Si. With charge trapping in the nanocrystals, the nanocrystal capacitance C_{nc} should decrease as the number of uncharged nanocrystals responding to the small AC signal in the C-V measurement is reduced. If all the chargeable nanocrystals are charged up, then C_{nc} should approach zero. Thus the MOS capacitance is very small as it is now determined by the remaining gate oxide capacitance C'_{ox} (<700 fF). On the other hand, if the charges trapped in the nc-Si are released, then C_{nc} should increase leading to an increase in the MOS capacitance. This explains the experimental results shown in Figs. 2 and 5.

4 CONCLUSIONS

In conclusion, MOS structures with nc-Si embedded in the oxide layers were synthesized by the ion implantation technique. It is found that nc-Si distribution has an effect on the MOS C-V characteristics: For the case of nc-Si confined in a layer in the oxide, even a small difference in the location of the peak concentration of nc-Si can yield a significant difference in the memory programming characteristics, while for the case of nc-Si distributed throughout the oxide with a high concentration, capacitance modulation can be obtained by charging/discharging nc-Si. The difference between the two cases highlights the importance of the nc-Si distribution in device applications.

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