# Tests of the Sigma-Delta Converter Designed as a Part of Microsystem Dedicated to Water Pollution Monitoring

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## ABSTRACT

In this paper a dedicated modular structure of a sigma-delta converter is presented. The described structure is a result of the research that has been undertaken during the 5th European Programme SEWING (System for European Water monitorING). The aim of this project was to elaborate a small, cheap and commonly obtainable microsystem, which task is to measure water pollution in European lakes and rivers. The main part of this system is a set of CHEMFET sensors, which were described in previous papers [2],[4]; the other part is a processing unit, which is based on an analogue to digital converter (ADC). At the start-up of the designing process it was assumed that the 12-bit ADC should have been elaborated, finally such a converter has been designed in AMS 0.6µm CMOS technology. In addition, the ADC structure was designed as a modular one [3],[5], so the order of the modulator can be easily changed from the 1st to the 4th order. The modular structure allows also for implementing the MASH structure into the real life project. The final result is the possibility of a choice among four different converter configurations. The design path of the ADC was divided into two major parts. In the first one, the model of the device was described in the VHDL-AMS language in which also a set of simulation was performed. During the second part, an electrical circuit was drawn and tested in CAD CADENCE environment; also the final version of the converter layout was prepared there. The ADC design path was further verified during tests of the manufactured chips. The results of the measurement are presented and discussed, as well as conclusions that are included in this paper.

***Keywords***: CAD CADENCE, MICROSYSTEM, SEWING, SIGMA-DELTA CONVERTER, VHDL-AMS

## 1 INTRODUCTION

The elaboration of the microsystem dedicated specially to the water pollution monitoring was one of the main features of the SEWING Project, which is a part of the 5th European Frame Programme. In this particular project, the five universities from all over Europe as well as two institutes and two commercial companies take part in.

The task of the Department of Microelectronic and Computer Science (DMCS) at Technical University of Lodz was to elaborate the microsystem, which consists of sensor and data processing part. The main part of the processing unit is the analogue to digital converter, which according to the project specifications, should be a 12-bit one. Two different converters were taken into consideration: a Successive Approximation ADC and a Sigma-Delta ADC, after a basic research the Sigma-Delta (ΣΔ) ADC was chosen. The model of the converter was described in the VHDL-AMS language, such an approach allowed for testing various configurations of the device in the very short time. Moreover it was possible to investigate the behaviour of the whole microsystem containing the CHEMFET sensors [2],[4] connected directly to the ADC. As a result of works on this stage, two most promising structures were chosen and implemented in the CAD CADENCE environment. The final layout of the ADC was elaborated in AMS 0.6µm CMOS technology. The manufactured prototypes were then tested in the DMCS. The measurement results compared with the simulations are the main objective of this paper.

## 2 SIGMA-DELTA CONVERTER MODELLING

In this section the model of ΣΔ converter is presented. The description in the VHDL-AMS language allowed for testing of various ADC configurations [6], what benefited in simulation time reduction, and choosing the most promising solution for the CAD CADENCE implementation. All ADC models consisted of basic components submodels, that approach allowed for design flexibility and possibility of different configuration verification. At the beginning the serial integrators connection, form 1st up to the 4th order, was taken into consideration, then also several cascade structures were tested. The block diagram of the second order ΣΔ modulator is presented in Fig.1.

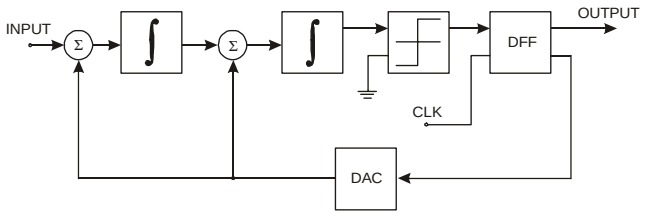


Fig.1. Second order sigma-delta modulator

To verify all models the static characteristics were drawn (Fig.2). As can be seen the transfer characteristics for all three tested models, from the 1st up to 3rd order ADC were linear. It also should be mentioned that functions describing integrators submodels were ideal ones, what resulted in ideal transfer characteristics.

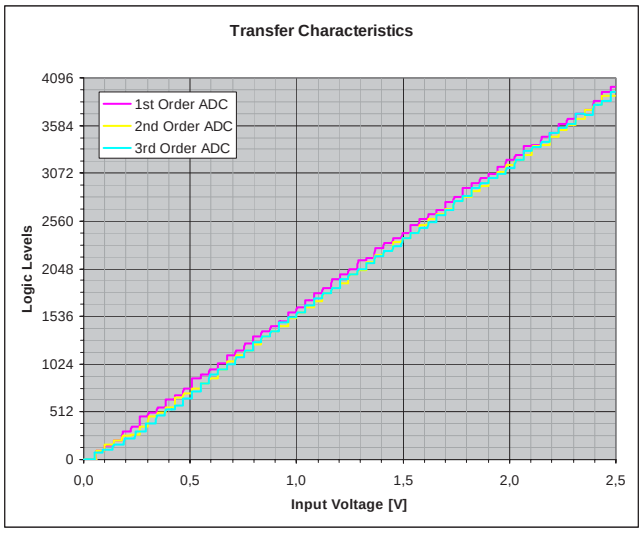


Fig.2. Transfer characteristics of VHDL-AMS models

All tests were performed also in the ideal conditions; the input of the ADC was applied with sinusoidal signal of the 1kHz frequency, which amplitude was equal to the full range of the converter. The output words were written into the ASCII file, and then converted into analogue again. Then the FFT of the output signal was calculated to estimate the harmonic distortion of the signal. As an example, the FFT of the 2nd order ADC output signal is shown in the Fig.3.

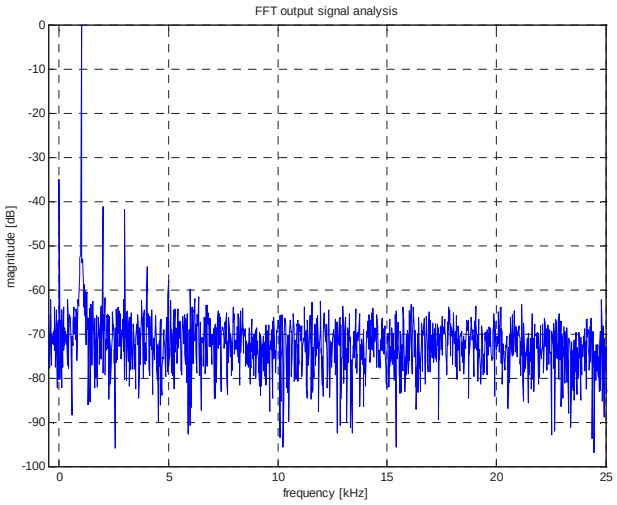


Fig.3. FFT of the output signal from 2nd order ADC (simulations)

The next step after modelling the ADC in the VHDL-AMS language was to implement the chosen structures in the CAD CADENCE environment. It was decided to elaborate the layout of the four serial integrators (from the 1st up to 4th order), and also the cascade structure well known as a MASH Triple First Order Cascade [1]. Circuit diagrams of the elaborated structures are shown in Figs 4 and 5 respectively.

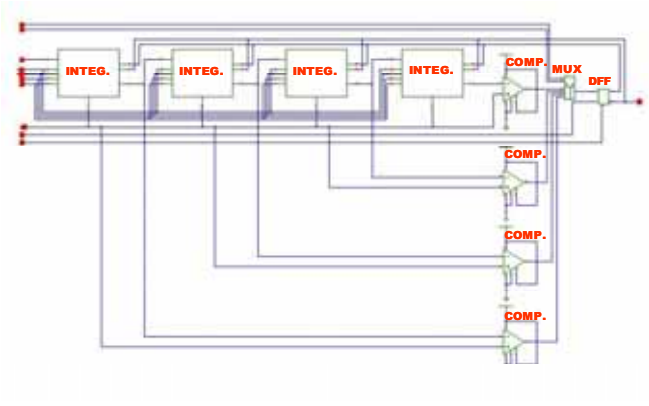


Fig.4. Circuit diagram of modular structure of serial integrators connection

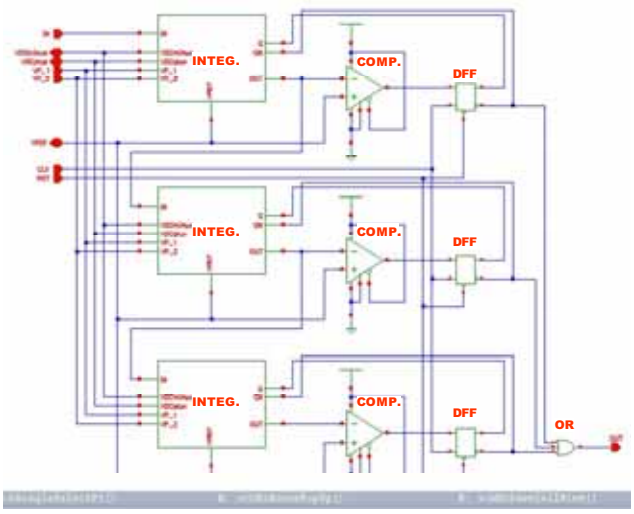


Fig.5. Circuit diagram of MASH structure

The last stage of the design was to develop the final layout of the converter in the AMS 0.6µm CMOS technology. The modular structure of the implemented device allowed for testing various configurations of the converter to choose the most adequate ADC for the developed water pollution monitoring microsystem.

The Prototype of the ADC (Fig.6) was manufactured in a silicon foundry as a stand alone chip, in the final version it will be an integral part of a whole microsystem. The chip area is 4.2mm$^2$.

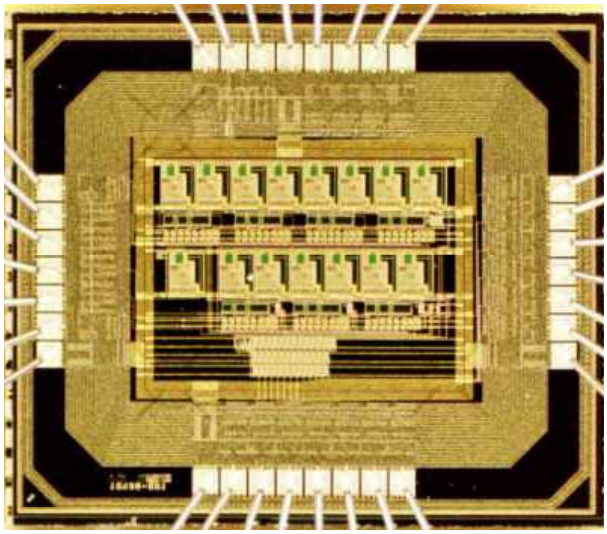

Fig.6. The ADC prototype photo under the microscope

## 3 MEASUREMENT STAND DESCRIPTION

The special measurement stand was elaborated to measure presented chip [7]. It consists of:

- Input signal generator
- Test board
- PC equipped with Data Acquisition Card

The designed test board allowed for the adjusting external clock frequency and the reference voltage. It contained analogue and digital buffers, which protect tested chip against undesired input voltage level. There were analogue RC low-pass filters (100kHz cut-off frequency) on the input. To generate clock signal the quartz oscillator, which works on the 3rd harmonic, was used. To adjust reference voltage the 8-bit analogue to digital converter was used. The heart of measurement stand was the described test board presented in Fig.7.

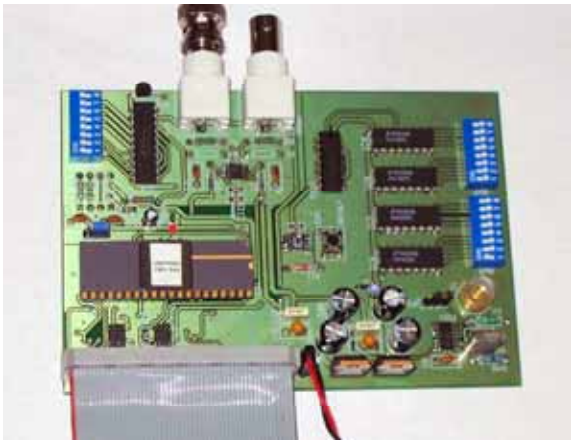

Fig.7. The test board photo

## 4 SIGMA-DELTA CONVERTER MEASUREMENTS

In this section results of the practical verification of the designed ΣΔ converter are presented. The measurements were divided into two parts:

- Static parameters
- Dynamic parameters

According to preliminary measurements, structures are presented as follows:

- 1st order ADC
- 2nd order ADC
- 3rd order ADC

The transfer characteristics of the other converters are not presented, because of their non-linearity, what eliminates these devices from practical implementation into the microsystem.

The ADC transfer characteristics obtained during static measurements of the prototype are shown in Fig.8.

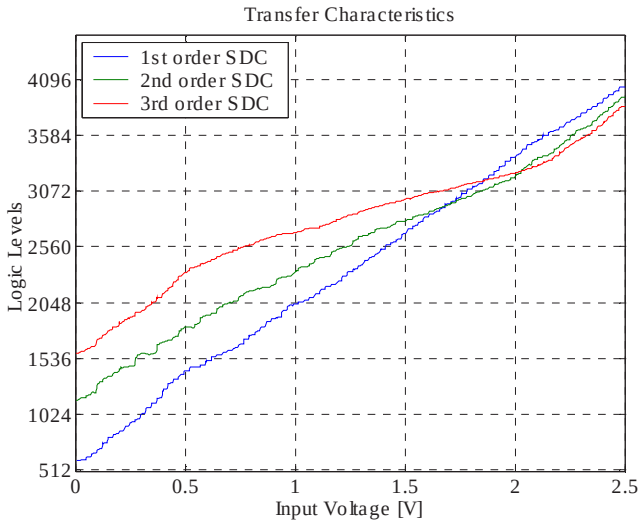


Fig.8. Transfer characteristics of the prototype

As can be seen in Fig.8 the most linear characteristic were obtained for the 1st order ADC. Unfortunately, the transfer characteristic of the 3rd order ADC, which was the most desirable, was not linear in the whole range, what made this particular structure inconvenient according to the project assumptions. In all structures an offset, which had to be compensated in the real life device, was noticed. But it is worth to say that the clock frequency in tested chip was 3MHz, and the positive reference voltage was 2.5V. The total power consumption was 32mW.

The second part of tests was devoted for estimating the dynamic parameters of the prototypes. To calculate the dynamic parameters, inputs of each converter were applied with the sinusoidal signal, the digital output words were saved in the ASCII file, and then the FFT of the output signals was performed. The next step was to calculate the Signal to Noise Ratio (SNR) and the Total Harmonic

Distortion (THD), which are presented in Tab.1. The exemplary FFT of the 2nd order ADC output signal is shown in the Fig.9.

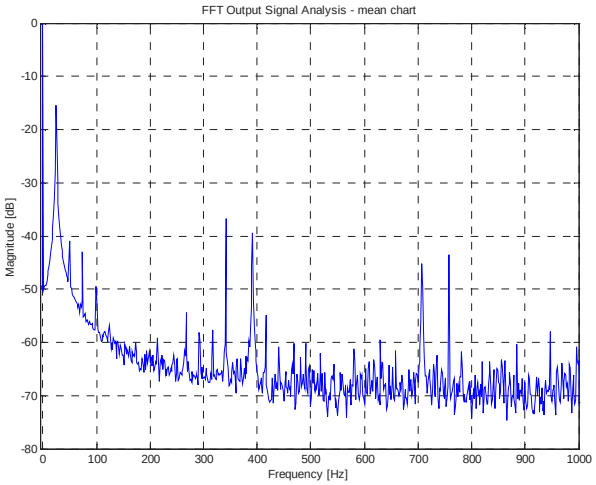


Fig.9. FFT of the 2nd order ADC output signal (measurements)

Tab.1. Dynamic parameters of the ADCs.

| Configuration of ADC | 1st order | 2nd order | 3rd order |
|---|---|---|---|
| Frequency [Hz] | 25 | 25 | 25 |
| SNR [dB] | 63.55 | 66.56 | 54.98 |
| THD [dB] | -18.99 | -18.80 | -14.18 |

As can be seen the best parameters were obtained for the 2nd order ADC. The parameters' values depended from the noise shaping in the converter. The noise level was decreased in the low frequency band, what resulted in much better SNR for the 2nd order ADC than for the 1st order ADC. To obtain better parameters in higher order of the ADC, it is necessary to optimize such converter individually.

## 5 CONCLUSIONS

The designing path and also the measurement of the prototype of the modular ΣΔ ADC was presented in this paper. The modular structure of the device allowed for adjusting the order of the modulator by using the digital multiplexer, to obtain the converter characterizing the optimal parameters for the designed microsystem. The results obtained during measurements positively verified the established in the project designed path, but also shown the problem of transfer characteristics for the upper ADC orders. The authors will continue research in this area, especially on the 16-bits converters.

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