The Modeling and Characterization of Nano-Scale MOSFET Resistance

Jun-Ha Lee[*], Hoong-Joo Lee[*], Woo-Hee Lee[*], Eu-Seok Kang[**], Ju-Yul Lee[**], Ki-Ryang Byun[**], Jeong-Won Kang[**], Ho-Jung Hwang[**] and Oh-Keun Kwon[***]

[*]Information Display Research Center, Department of Computer System Engineering, Sangmyung Univerisity, Chonan, Korea, junha@smu.ac.kr
[**]School of Electrical and Electronic Engineering, Nano Electronic Future Technology Laboratory, Chung-Ang University, Seoul, Korea, gardenriver@korea.com
[***]Department of e-Commerce, Semyung University, Jecheon, Korea, kok1027@semyung.ac.kr

ABSTRACT

The current drive in an MOSFET is limited by the intrinsic channel resistance. All the other parasitic elements in a device structure play a significant role and degrade the device performance. These other resistances need to be less than 10%-20% of the channel resistance. To achieve the requirements, we should investigate the methodology of separation and quantification of those resistances. In this paper, we developed the extraction method of resistances using calibrated TCAD simulation. The resistance of the extension region is also partially determined by the formation of a surface accumulation region that forms under the gate in the tail region of the extension profile. This resistance is strongly affected by the abruptness of the extension profile because the steeper the profile is, the shorter this accumulation region will be.

Keywords: parasitic resistance, methodology, separation, quantification, extraction

1 INTRODUCTION

In recent high density silicon devices, local properties caused by such as dopant density variation, structural and chemical uniformity of the dielectric layer affect the stability and reliability of the device operation [1]. With sizing effect, local dopant density variation also affects the characteristics and performance of the devices [2].

Ideally, the driving current of the MOSFET is controlled by the channel resistance, but the other resistive components, realistically, are major causes of the performance deterioration of the device [3]. So far, many studies have been done on the doping profiles and device structure to minimize the intrinsic and parasitic resistance in the MOSFET structures. However, they mostly use the mobility enhancement of carrier as a main control factor; therefore they only give the information on channel engineering. The parasitic resistance and capacitance bringing about both the lowering of the current driving and the increment of the node capacitance, consequently have an effect on the CMOS delay. It has been reported that both the shallow junction and the heavily doped extension as the methods to minimize the off-current and to stabilize the on-current of the sub-90nm scaled device, can solve the short-channel effect and manufacturing difficulties [4-5]. In this study, the performance improvement for the high speed and high performance device has been presented through the resistance study using TCAD(Technology Computer Aided Design) simulation. The proposed method make it possible to extract effectively the optimized process window by analyzing the relation between the process parameters and parasitic resistance and through the sensitivity analysis of the parasitic resistance in each region of the device.

2 PRINCIPLE AND METHOD

2.1 Calculation of Parasitic Resistance

There are five resistive components and current flows which must be considered in MOSFET devices [6]. As the decrease of the source current make drop the gate driving ability, the source region must be thoroughly analyzed. Among five resistive components, ① to ④ are parasitic resistances and each is classified as the contact resistance, the shunt resistance, the extension resistance and the accumulation resistance. ⑤ is the intrinsic channel resistance. The sheet resistance of each region is extracted by the eq. (1) [7]. The current and quasi-fermi potential was used from the simulation results. From the eq.(1), we can get the value of sheet resistance each node point along the x-axis.

$$I_{ds} = \int_0^\infty J(y)dy = \frac{d}{dx}\phi_n(x)\int_0^\infty qn(x,y)\mu(x,y)dy = \frac{\frac{d}{dx}\phi_n(x)}{R_{sh}(x)} \qquad (1)$$

,where x is the horizontal scale, Φn or Φp are electron/hole quasi-Fermi potentials, and Ids is the total current.

2.2 Process and Device Simulation

To extract the substantial current values and quasi-fermi level in each region for the given process condition [8], the simulator calibration must be preceded in order that the results from the process and device simulation has the same doping level and the mobility value as those of the real device. In this paper, n/pMOS devices of which source/drain activation has been done by normal-RTA(Rapid Thermal Annealing) and spike-RTA, have been used as the targets of the calibration [9-10].

Fig. 1 shows the comparison between simulation results and measures of Lgate(Gate Length) versus Vth(Threshold Voltage). The results from the TCAD simulation show a good agreement with the electrical characteristics of the real device, based on the comparison between the simulation and measure for correlation of Idsat versus Ioff in Fig. 2. The solid lines in Fig. 1 and Fig. 2 represent measurement values for the real device, and the dotted lines describe the simulation values. The error between measure and simulation has been less than 10% for n/pMOS to which both the spike-RTA and normal-RTA have been applied. The error between measure and simulation for Idsat-Idoff curve from the short-channel region of the device to which the only normal-RTA have been applied, have been more than 10%.

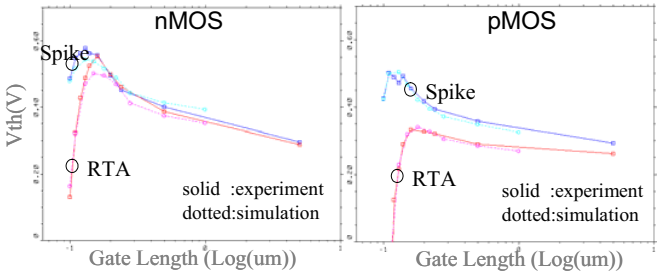

Figure 1: The Lgate-Vth curve from TCAD simulation.

(a) nMOS (b) pMOS

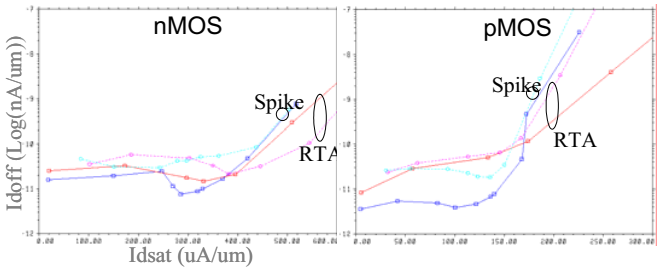

Figure 2: The Idsat-Idoff curve from TCAD simulation.

(a) nMOS (b) pMOS

2.3 Separation and Quantification of Resistance

Fig. 3 shows the extracted sheet resistance for x-axis position for the nMOS device. The line represents the spike-annealed process, and the symbolled line represents the normal-RTAed process. The junction contours for each process are depicted using the dotted lines. 25% shallower junction depth of 750 Å for the case of spike-RTA has been obtained compared to 1000 Å junction depth for the normal-RTA. The proposed five resistive regions can be easily separated considering carefully the junction contour and the gate edge. The extracted resistance values from Fig. 3 are tabulated into table 1 and table 2. The spike-RTA shows the bigger total resistance compared to the normal-RTA due to the incomplete activation with the shallower junction depth [11-12]. For both cases, the parasitic resistance is about 15% of the total resistance. Moreover, it is 17% of the channel resistance, which is similar to that introduced in ITRS [13].

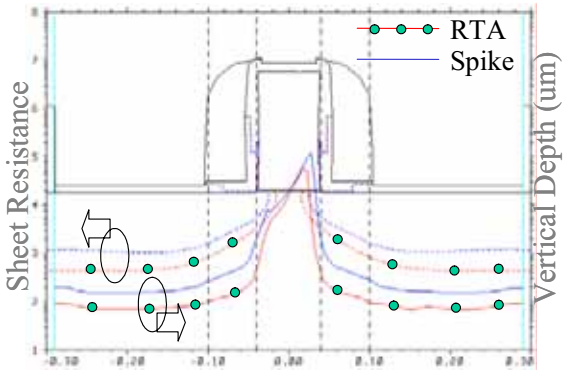

Figure 3: Junction contour and sheet-resistance of nMOS.

Fig. 4 shows the doping contour and the sheet resistance for the normal-RTA annealed pMOS device. The red contour lines represent the same doping concentration, and for the case of the pMOS device, the extension region is not shown to be indistinguishable from the source/drain region. Futhermore, The reason why the junction of the extension region of the pMOS device is deeper than that of nMOS device is that it is difficult to make the shallow and abrupt doping profiles due to the TED (transient enhanced diffusion) for the boron impurities [14]. The simulation value of the junction depth is about 1200 Å. Parasitic resistances are also separated according to the separated regions shown in figure 4. The green line represents the steep increase of sheet-resistance in the accumulation region, which means the parasitic resistance increases in proportion to the length of the accumulation region [15]. In case of pMOS, the parasitic resistance forms about 23% of the total resistance, and also comes to 30% of the channel resistance shown in table 3. The spreading resistance is about 18% of the total resistance. Since 65% of the parasitic

resistance is Racc(Accumulation Resistance) which is analyzed in table 4, the parasitic resistance value is found to be quite high. Because the boron profile in the tail region is not abrupt enough, the excessive overlap under the gate has the accumulation resistance increased [16]. Therefore, the parasitic resistance can shrink into its half similar to the case of nMOS, if the Racc, 15% of the total resistance, is half decreased.

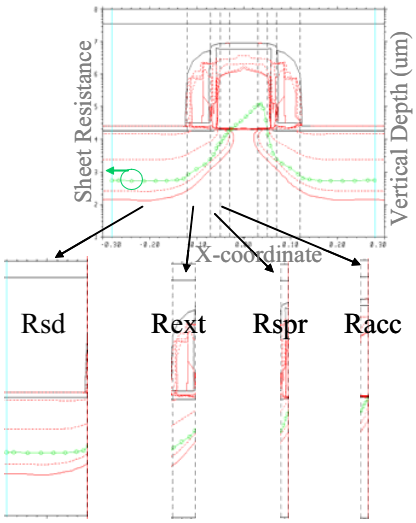

Figure 4: Junction contour and sheet-resistance of pMOS.

Table 1: Resistance component of RTA-annealed nMOS.

nMOS RTA-anneal	Percentage (%)	Resistnace value (Ω)
Total Resistance	100	1041
Channel Resistance	86	892
Parasitic Resistance	14	149
Accumulation Resistance	5	50

Table 2: Resistance component of Spike-annealed nMOS.

nMOS Spike-anneal	Percentage (%)	Resistance value (Ω)
Total Resistance	100	1847
Channel Resistance	85	1574
Parasitic Resistance	15	273
Accumulation Resistance	4	71

Table 3: Resistance component of RTA-annealed pMOS.

pMOS	Percentage (%)	Resistance value (Ω)
Total Resistance	100	489
Channel Resistance	77	376
Parasitic Resistance	23	113

Table 4: Analysis of the resistance in parasitic region.

pMOS Parasitic Resistance	Percentage (%)	Resistance value (Ω)
Shunt(S/D) Resistance	2.2	11
Extension Resistance	2.0	10
Spreading Resistance	3.8	18
Accumulation Resistance	15.0	74

2.4 Analysis of the Contact Resistivity

Cobalt-silicide/silicon contact resistance is expected to be a large portion of the parasitic resistance. The current flows on the distributed paths from the extension to the contact, and the exact path depends on the doping profiles and the device structure. The effective contact resistance is thus effected by the current flow lines, and effective contact area of silicon and cobalt. As silicidation consumes silicon atoms, the highly doped source/drain region could disappear or be located in the silicide area. In this case, the resistivity of the silicide or the highly doped silicon region depends on the doping level in the adjacent region to the silicide [17]. In Fig. 5, the contact resistivities of the n/pMOS devices have been calculated. The source/drain doping levels must be kept up more than 1E20 for the nMOS and 6E19 for the pMOS respectively to be in compliance with the ITRS standard.

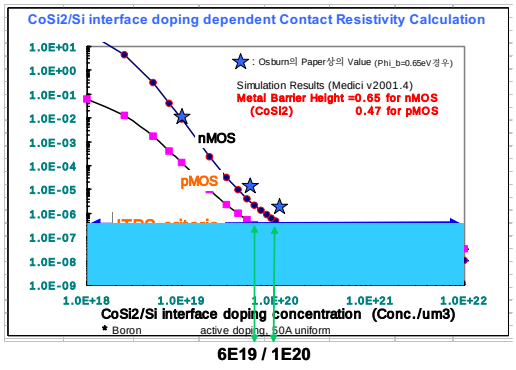

Figure 5: The contact resistivity depend on adjacent silicon doping concentration level.

The doping level in the silicon near the cobalt silicide has been analyzed using the SIMS(Secondary Ion Mass Spectroscopy) measurement. As shown in Fig. 6, for the pMOS, the severe segregation of boron impurities occurs in the silicon region adjacent to the cobalt silicide, which becomes more serious with the higher temperature of silicidation. Therefore, the initial ion-implantation energy, silicidation process condition, and the silicide thickness should be optimized to minimize the contact resistance. Additionally, the cross-sectional area of the current path must be maximized.

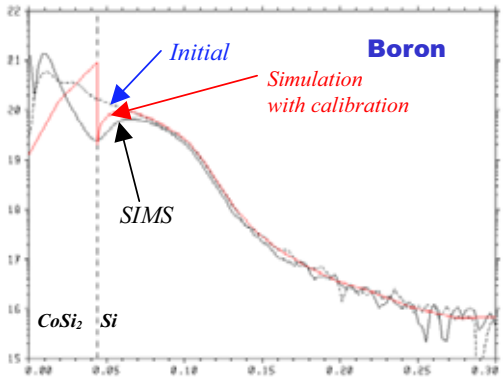

Figure 6: Doping level of adjacent to the Co-silicide.

3 CONCLUSION

This paper has analyzed the resistive components of the contact which lowers the device performance. A flow has been proposed to obtain the sheet resistance at each node with the current values and quasi-Fermi levels calculated by the calibrated TCAD simulation. The rate between the channel resistance and the parasitic resistance as well as four parasitic resistive components and their relation for the normal and spike-RTA annealed n/pMOS devices, has been extracted to find optimized process condition. Also, this work has presented the methods to optimize the contact resistivity depending on the doping level in the silicon adjacent to the cobalt silicide region. The proposed method can make it possible to obtain effectively the process window to minimize the parasitic resistance for the high speed devices.

REFERENCES

[1] C. J. Kang, D. Jeon and Y. Kuk, Surface Science, **544**, 87 (2003).

[2] R. J. Luyken, T. Schulz, J. Hartwich, L. Dreeskornfeld, M. Stadele and W. Rosner, Solid-State Electronics, **47**, 1199 (2003).

[3] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI De-vices. Cambridge, MA: Cambridge Univ. Press, 1998.

[4] Y. Taur, IEEE Trans. Electron Devices, **47**, 160 (2000).

[5] S.D.Kim, C.M.Park and J. Woo, IEDM'00 pp.723-726. (2000).

[6] K. K. Ng and W. T. Lynch, IEEE Trans. Electron Devices, **33**, 965 (1986).

[7] M. Y. Kwong, C. H. Choi, R. Kasnavi, P. Griffin and R. Dutton, IEEE Trans. Electron Devices, **49**, 1324 (2002).

[8] P. Degond and A. El Ayyadi. A Coupled Schrodinger, Journal of Computational Physics, **181**, 222 (2002).

[9] J.H. Lee, et. al., MSM'00, pp. 89-93 (2000).

[10] A. La Magna, S. Coffa, S. Libertino, Matthias Strobel and L. Colombo. Computational Materials Science, **24**, 213 (2002).

[11] L. Ihaddadene-Le Coq, J. Marcon, A. Dush-Nicolini, K. Masmoudi and K. Ketata. **216**, 303 (2004).

[12] Giovanni Mannino, Vittorio Privitera, Sandro Solmi and Nicholas E. B. Cowern. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, **186**, 246 (2002).

[13] International Technology Roadmap for Semiconductors:(ITRS) SEMATECH, Austin, TX, (2001).

[14] N. Fujiwara, K. Saito, Y. Nakabayashi, H. I. Osuman, K. Toyonaga, S. Matsumoto and Y. Sato. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, **186**, 313 (2002).

[15] J. O. Borland, Mat. Res. Soc. Symp. Proc. **717**, C1.1.1, (2002).

[16] A. Dusch, J. Marcon, K. Masmoudi, K. Ketata, F. Olivie, M. Benhzora and M. Ketata. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, **186**, 360 (2002).

[17] C.M. Osburn, K.R. Bellur, Thin Solid Films 332, **428** (1998).