Mismatch Improvement with XMOS Structure

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ABSTRACT

In this paper, we present how mismatch can be improved by changing the structure of the MOS transistor. The structure that we proposed is Cross MOS (XMOS) structure. By constructing the gate structure in a cross shape, both the transistor performance and the transistor mismatch can be improved at the same time.

Keywords: mismatch, cross MOS, XMOS, cross gate, analog circuit.

1 INTRODUCTION

MOS transistor has been continuously scaled down to improve the device performance. Smaller MOS transistors have higher transconductance (gm) and low capacitance, so the ratio gm/C is improved by shrinking. Shorter gate length provides higher drain current which improve the transistor switching speed. Mismatch is one of the major barriers for device downscaling, especially for analog designers.

Mismatch and transistor size always contradict each other. From inverse square root area law, mismatch increases when transistor size decreases. This means that it is almost impossible to improve the transistor performance (by shrinking the gate length) and to improve the transistor mismatch at the same time.

In this paper, we propose a method of constructing the gate structure that will improve both the transistor performance and the transistor mismatch at the same time. The structure that we proposed is Cross MOS (XMOS) structure. The XMOS structure has a cross gate that provides extra channel width that gives higher transistor performance and extra gate area that provide better transistor matching. But there is no increase in source/drain parasitic capacitance [1].

We have shown the design of XMOS structure in [2]. A 90 degree rotated poly line is added to the original poly line of the conventional MOS structure to form the XMOS transistor structure. XMOS structure has advantages over the existing enhance transistor structures, such as, finger MOS transistor, annular transistor [3] and Waffle transistor [4, 5], in terms of smaller parasitic source/drain junction capacitance, ease of use and suitable for applications where minimum size transistors are required.

We also demonstrated that by converting the conventional MOS to XMOS, the transistor switching speed can be improved by 12.3% [6]. This result is verified by measuring the output frequency from two inverter ring oscillators. One employed the XMOS transistors and the other with the conventional transistors.

This paper will concentrate on the mismatch behavior of XMOS transistor that makes this structure an ideal choice for analog design such as current mirror or differential matched pair. The symmetrical shape of the XMOS structure is also believed to contribute better matching behavior [7] besides of the larger gate area.

2 EXPERIMENT

In this experiment, different sizes of XMOS transistor pairs, as shown in Figure 1(a) and standard transistor pairs as shown in Figure 1(b), are drawn and fabricated using Silterra 0.18um CMOS process. All the transistor sizes are specially chosen to get the inverse square root area plot.

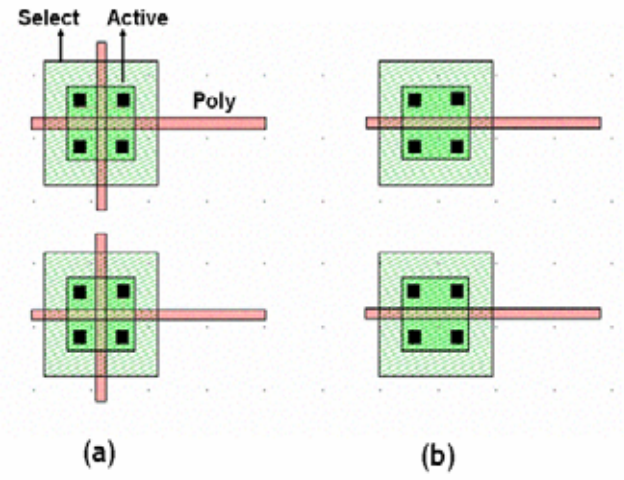

Figure 1: (a) XMOS transistor pair (b) Standard MOS transistor pair.

The electrical parameters, threshold voltage at linear and saturation regions (Vtlin and Vtsat), and drain current at linear and saturation regions (Idlin and Idsat) are measured from the transistor pairs. Vtlin mismatch is the standard deviation of the difference in Vtlin between the transistors in a pair. From the inverse square root plot, Vtlin

mismatch coefficient, A_{Vtlin} is calculated from the slope of the line. The mismatch of Vtsat, Idlin and Idsat are calculated in the same way as Vtlin.

In this experiment, the number of sample is 32, which is the number of dice in the one wafer that we used. Linear condition is defined as Vd=0.1V and saturation condition is defined as Vd=1.8V. The threshold voltage, Vt is taken as Vg at Id = 0.1uA*W/L.

3 RESULTS AND DISCUSSION

The mismatch plots of Vtlin, Vtsat, Idlin and Idsat for comparing XMOS and Standard MOS (Std MOS) are shown in Figure 2, Figure 3, Figure 4 and Figure 5. These plots are taken from the PMOS data. In our study, NMOS mismatch shows similar characteristics as PMOS in making comparison between XMOS and Std MOS. Hence, we only show the PMOS data in this paper.

From Figure 2 to Figure 5, we can see that XMOS mismatch and Std MOS mismatch fall into the same line in the inverse square root plots. This means that both the XMOS and Std MOS have the same mismatch coefficient. Thus, the mismatch improvement by converting Std MOS into XMOS is mainly contributed by the extra gate area gained.

We believe that the symmetrical shape of the XMOS transistor also contributes to better matching instead of the extra gate area gained. We are not seeing it in the plots because the mismatch improvement from the symmetrical shape is too small if comparing to the mismatch improvement gained from the larger gate area. The mismatch coefficient will be different (smaller) if there is any other significant contribution to the better matching instead of the gate area.

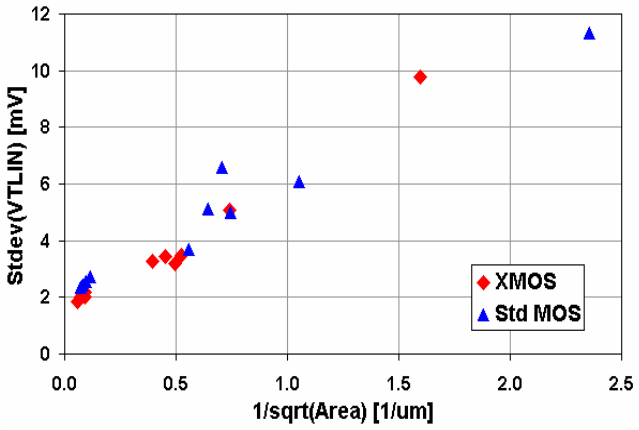

Figure 2: Vtlin mismatch plot for comparison between XMOS and Standard MOS.

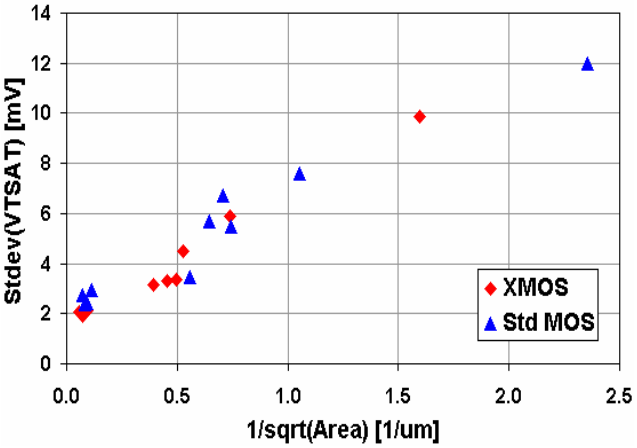

Figure 3: Vtsat mismatch plot for comparison between XMOS and Standard MOS.

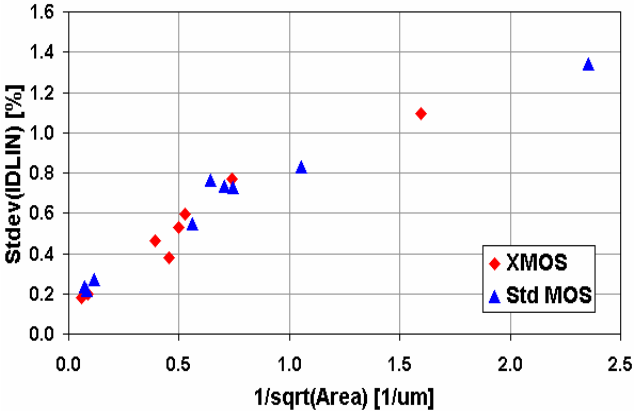

Figure 4: Idlin mismatch plot for comparison between XMOS and Standard MOS.

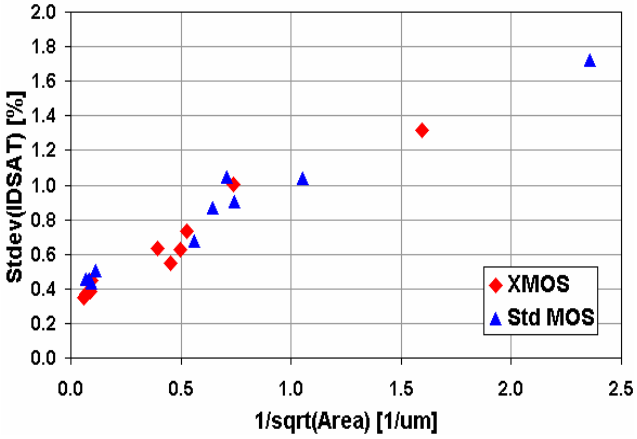

Figure 5: Idsat mismatch plot for comparison between XMOS and Standard MOS.

For illustrating how much mismatch improvement can be achieve by applying the XMOS structure, we take an example of the Std MOS with W/L=1.18/0.18. By adding an extra poly line crossing the gate and the active is in square shape, we can form a XMOS with W/L=2/0.18. Figure 6 and Figure 7 show the amount of Vtlin and Idsat mismatch improvement we can gain from this conversion.

By applying XMOS structure to 1/0.18 Std MOS device the Vtlin mismatch improves 1.6mV (from 11.3mV to 9.7mV) as shown in Figure 6 and the Idsat mismatch improves 0.4% (from 1.7% to 1.3%) as shown in Figure 7. Of course, converting the 1/0.18 Std MOS device to a two-finger transistor with W/L=2/0.18 also can achieve about the same mismatch improvement due to larger gate area, but we have to use larger active area which means the transistor size will be increased, along with the parasitic capacitance.

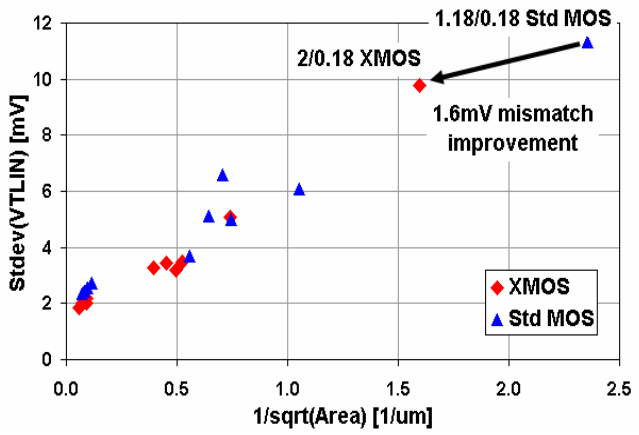

Figure 6: Amount of Vtlin mismatch improvement achieved by converting Standard MOS to XMOS.

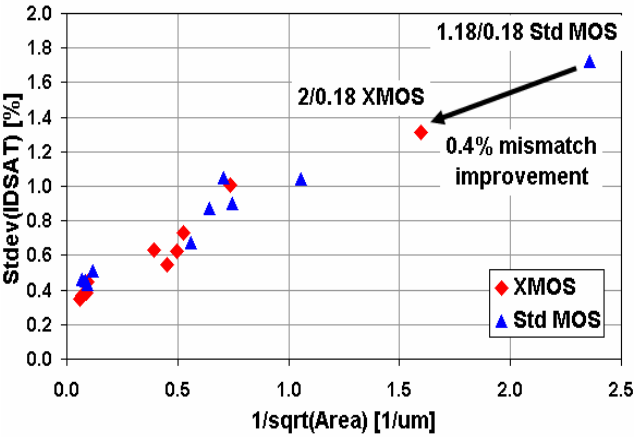

Figure 7: Amount of Idsat mismatch improvement achieved by converting Standard MOS to XMOS.

For Std MOS with 0.18um in length and width equal or larger than 1um, we can approximate the amount of gate area gained is about 2X. From this approximation, we derived an equation to calculate the amount of mismatch gained by converting Std MOS into XMOS, as shown in Equation (1).

$$\Delta_{Mismatch} = \left(\frac{0.293}{\sqrt{W \cdot L}} \right) A \qquad (1)$$

where W is the transistor width, L is the transistor length and A is the mismatch coefficient.

The Equation (1) will hold for Std MOS devices with W/L ratio larger than 5 and with square shape active area. By using this equation, we can decide whether we are able to achieve the required mismatch by converting the Std MOS to XMOS structure.

4 CONCLUSION

The main purpose of this paper is to provide an insight of how to improve both transistor performance and transistor mismatch at the same time by just modifying the MOS transistor layout style. Another way to improve both factors together would be shrink the device but employ an excellent process capability, which would involved extreme high cost. We hope this paper will give analog designers an alternative way of drawing transistor layout that will improve their circuit performance.

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