Wafer scale aligned sub-25nm metal nanowires on Silicon (110) using PEDAL lift-off process

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ABSTRACT

We have demonstrated a new PEDAL process to make sub-25 nm nanowires template across the entire Silicon (110) wafer suitable for wafer-scale nanoimprinting. The "PEDAL lift-off" has the ability to fabricate metal nanowires directly on the wafers without using nanoimprint techniques. The process involves defining the edge by etching a trench, patterned using conventional i-line lithography, and followed by deposition of alternating layers of silicon nitride and a-silicon. The thickness of these layers determines the width and spacing of the nanowires. Later this stack is planarized to the top surface of the trench by spinning polymer and then dry etching the polymer, nitride and a-silicon stack with non-selective RIE etch recipe. Selective wet etch of either nitride or a-silicon gives us the template of array of aligned nanowires. The desired metal is evaporated by e-beam on the template and metal deposited on a-silicon layer is lifted-off by wet-etching a-silicon layer. This gives us the metal nanowires deposited on the insulating silicon nitride layer across the wafer. The process has the flexibility of routing the nanowires around the Logic and memory modules across the entire wafer. The fabrication facilities required for the process are readily available and this process provides the great alternative to existing slow and/or costly nanowire patterning techniques. PEDAL lift-off process when incorporated with Atomic Layer Deposition has the ability to make wafer-scale aligned sub-5 nm wide nanowires.

Keywords: Nanoimprinting, Mold, Template, Interconnects, Nanotechnology, Lift-off, Nanowires, Planarization

1 INTRODUCTION

In microelectronics where the critical dimensions of interconnects shrink with the continuous trend to downscale the size of semiconductor devices such as IC and memory cells, nanowires present an important application. There are various methods for fabricating patterned nanowires, but organizing these wires into highly ordered arrays with predetermined spacing and registry has been extremely challenging [1] [2]. The methods to fabricate nanowires are (1) lithography with photons in UV, DUV, EUV, and X-ray spectrum (2) lithography using electron, ions and neutral atoms (3) machining using AFM, STM, NSOM (4) replication against masters(or molds) via physical contact printing, molding and embossing (5) self assembly by using surfactant systems, block copolymers, crystallization of proteins, and colloids (6) spacer formation, controlled deposition and size reduction, and shadowed/oblique evaporation on surface through a mask (7) Isotropic deformation processes by the compression of elastomeric masters or molds(8) SNAP process involving multiple epitaxial growth of alternate material and using cross-section of such stack as a nanowire template. Each of these methods has some basic intrinsic limitations and in recent years much research has been done to overcome these limitations to achieve sub-50nm features. In photon based lithography by using nonlinear resists, near-field phase-shifting or topographically directed technology it has been possible to achieve sub-50nm feature. High cost, limited availability, low throughput and uniformity are still major issues with these nanowires patterning technology. In microcontact printing [3], micromolding [4][5],embossing and nanoimprinting techniques[6] [7], issues limited by vander-waals forces, speed of capillary filling and adhesion of mold and replica are overcome by using low viscosity solutions and surface modification. Although such methods may translate the serial method of EBL/EUV into a parallel patterning process, the mold formation still depends on EBL/EUV and its use restricted by high cost of molds. Immersion lithography has the potential to extend 193nm - ArF exposure systems to 45nm line-widths, and 157nm - F_2 systems to <30nm. Considering the significant issues still to be resolved with all of the post optical "Next Generation Lithography" tools, immersion lithography may prove to be

an essential tool for extending optical lithography through the end of the decade. SNAP process which is similar to nano-imprinting but without lift-off has demonstrated 8nm nanowires with 16 nm pitch [8]. However the template is formed on the edge of the wafer and its usability for patterning wafer scale nanowire structure and the alignment with previous layers of processing is yet to be demonstrated. It's also difficult to rout nanowires on wafer using SNAP. We have demonstrated in our current effort a challenging "Planar Edge Defined Alternate Layers (PEDAL)" process, which can be developed into more reliable technology to be used for wafer scale fabrication of sub-10 nm nanowires and templates.

2. OVERVIEW OF CONCEPT

PEDAL process involves defining the path and location of nanowires by etching a trench in silicon (110) wafer as shown in fig. 1(a) or in a layer deposited on the silicon wafer. After defining the trench, a conformal layer of amorphous silicon is deposited as a buffer layer as shown in fig. 1(b). Later, conformal alternate layers of silicon nitride and amorphous silicon are deposited on the wafer as shown in fig. 1(c). The wafer is spin coated with polymer to planarize the wafer surface as shown in fig. 1(d). The stack of polymer, silicon nitride and amorphous silicon is planarized to the top of buffer a-silicon surface using the non-selective etch process as shown in fig. 1(e). The nanowire template is obtained by etching a-silicon layer by a highly selective wet etch recipe. This gives the template which can be used for nano-imprinting. Fig 1(f) shows the nanowire structure obtained by selectively wet etching silicon nitride layer. To define nanowires directly on the wafer, desired metal is e-beam evaporated on the template as shown in fig. 1(g) and metal on top of the a-silicon layer is lifted-off by selectively wet etching a-silicon layer as shown in fig. 1(h).

3. EXPERIMENT

All the fabrication was done on p-type (110) Silicon wafer. The wafers were cleaned by soaking in acetone and methanol solution for 10 min each. The wafers were then cleaned with JTB-111 solution for 10 minutes followed by DI water rinse. 1300A silicon nitride film was deposited in a standard, horizontal hot wall LPCVD at 300 mtorr and 775 C using 40 sccm DichloroSilane and 120 sccm Ammonia for 40 min. The nanowire route was etched into this silicon nitride mask layer by defining line-width patterns of widths varying from 5 to 10 um using i-line lithography (365 nm). These lines were aligned along major wafer flat i.e. axis where {111} plane intersects the (110) plane at right angle. The trench to the depth of 1.8 um was etched into the silicon (110) wafer by using 40 wt % KOH solution at 80 C. This wet etch gives very smooth and vertical trench side walls due to the high selectivity of the

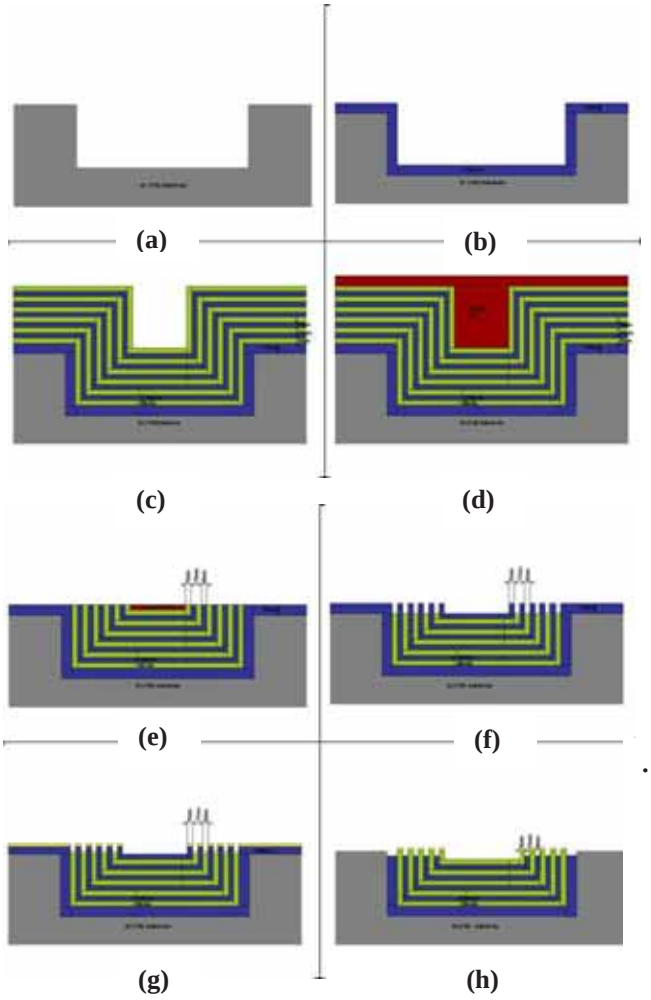

Figure 1: Process diagram for fabrication of nanowire template and nanowires using PEDAL lift-off process

KOH etchant on crystallographic {110} silicon plane over crystallographic {111} plane. The silicon nitride layer was etched off and the wafers were cleaned in JTB-111 solution for 10 minutes followed by DI water rinse. A 100 nm thick buffer layer of amorphous silicon is then deposited on the wafer in a-silicon LPCVD furnace at 130 mtorr pressure and deposition temperature 550 C using 60 sccm silane. Silicon nitride with average film thickness of 25 nm was deposited on the wafers in a horizontal hot-wall LPCVD system at 300 mtorr and 775 C using same recipe as described before. The wafers were later put in a-silicon LPCVD furnace to deposit 22 nm (average) of a-silicon film. The wafers were then left in ambient conditions in order to grow native oxide which prevents silicon atom diffusion on the amorphous silicon surface during annealing. After this, the wafers were put in nitride LPCVD furnace where the initial ramp-up time causes the solid phase crystallization of the a-silicon layer. The silicon nitride film of 25 nm average thickness is deposited and then wafers are put back in the a-silicon LPCVD. The

process is repeated a number of times depending on the number of nanowires.

After depositing the alternate layers of silicon nitride and a-silicon, the trench is planarized. Planarization is done by spinning organic polymer and etching the polymer, silicon nitride and a-silicon in RIE system by a non-selective etch recipe. For this purpose Shipley 1813 was spun over the wafer at 1500 rpm for 40 sec and later baked at 115 C for 10 minutes. The average thickness of the spun polymer is 2440 nm, giving good trench fill and surface planarization. Top 2300 nm of polymer was etched off by RIE using SEMIGROUP 1000 system at 30 mtorr pressure and RF power of 100 W using 15 sccm O_2 and 15 sccm SF_6. Later the non-selective etching is carried out till the stack is planarized with the top surface of buffer amorphous-silicon layer. The non-selective etch process is done at 30 sccm with RF power of 100 W using 5 sccm SF_6, 88 sccm Ar, 24.5 sccm CHF_3 and 2 sccm O_2. After planarization remaining polymer is removed by Nanostrip. The wafers were then soaked in acetone and methanol solution for 10 minutes each. The nanowires were created by selectively wet etching either a-silicon or silicon nitride. The silicon nitride nanowire template is created by selectively wet etching a-silicon. The average line-width obtained is 25 nm with average spacing of 22 nm as shown in the SEM in fig. 2(d).

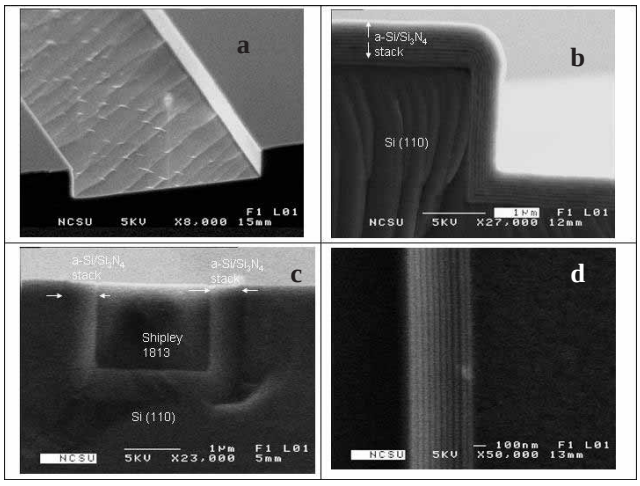

Figure 2: *SEM image* **(a)** 1800 nm deep trench etched into silicon (110) **(b)** Stack of alternate layers of a-Silicon and Silicon Nitride deposited by LPCVD **(c)** Planarization of stack and polymer to the top surface of the trench **(d)** Top view of template of array of 10 nanowires fabricated by PEDAL process.

4. RESULTS AND DISCUSSION

The fabrication was carried out on batch of 5 wafers, all of which showed good uniformity in nanowire width and spacing all across the wafer. It was possible to fabricate nanowires template with width as small as 25 nm using PEDAL process. The process provides the flexibility of routing the nanowires around the logic or memory modules of the circuit across the entire wafer. The template can also be used in conjunction with oblique metal evaporation and pattern transfer, or as the mold in wafer scale nano-imprinting to fabricate the wafer scale aligned nanowire structures.

We start with a pattern that is produced by photolithography and has spatial definition of the wavelength of the order of visible light (~ 600nm). The process depends on the i-line lithography to define the initial trench structures. These trenches in turn define the position of array of nanowires as well as the length of nanowires. The depth of the trench , as well as width of the trenches are decided after choosing the number of nano-wires, the required width of nanowires to be fabricated along the edge, and the spacing between these nanowires. The relation between the depths of the trench **d**, width of the trench **w**, number of nanowires **n**, width of nanowires $\mathbf{w_n}$, spacing **s,** is given by simple formula shown below (considering 100 nm of buffer layer)

$$d \geq n *(w_n + s) + 100nm$$
$$w > 2*n* (w_{n+} s) + 200nm$$

Above formula holds, assuming step angle of trench is 90 and the deposited materials is 100 % conformal. Modification in design is needed in order to incorporate deviation from ideal behavior. The fundamental limitation on the minimum width of nano-wires is the minimum thickness and conformality of the deposited materials as well as the step angle of trench.

Trenches were etched into silicon (110) wafer using 40% by weight KOH solution at 80 C. Anisotropicity of the wet etch using 40 %KOH is due to the selective etching of {110} planes to {111} planes. The family of {111} plane intersects {110} planes at right angles along two axis on a given (110) Silicon wafer. So it's very important to align the trench edges along these axes to get smooth vertical sidewalls. Fig. 2(a) shows the trench profile obtained by etching the trench aligned to <1, -1, -2> direction. The smooth vertical walls of trench are (1 -1 1) planes.

Films of controlled width were deposited using LPCVD process as it gives better conformality than MBE, PECVD, APCVD, PVD processes [18] [19]. LPCVD process used for depositing silicon nitride is a slow process with deposition rate of 32 A/ min at 775 C and hence it's possible to grow thin films of thickness less than 15 nm with great uniformity, repeatability and with surface roughness less than 3 Angstroms. Reducing the temperature can give even lower deposition rate and hence even smaller nanowire width. Amorphous silicon LPCVD is used instead of polysilicon because depositing a-Silicon on top of silicon nitride has provided films with surface roughness less than 5 Angstroms with great uniformity in thickness across the wafer. It was found that a-Si deposition at 500 C followed by 10 min RTA at 700 C provides film with thickness less than 10 nm [9] suitable to fabricate sub-10 nm wide

nanowires using PEDAL. Amorphous silicon and silicon nitride films deposited by LPCVD are highly conformal as shown in fig. 2(b). The uniformity in the thickness of these films deposited by LPCVD process is better than 3 % across the entire 4 inch wafer. We expect the same uniformity in the width and the spacing of the metal nanowires fabricated by PEDAL lift-off process.

The planarization process decides the uniformity of the height of nanowires across the wafer. We were able to demonstrate the planarization of stack of silicon nitride, a-silicon and Shipley 1813 using non-selective RIE process with 2.1 % uniformity in the etch rates across the 4 inch wafer. The etch selectivity observed was 1:1.05:1.00 for silicon nitride, a-silicon and polymer. The cross-section of planarized stack is shown in fig. 2(c)

The SEM of the structure obtained after etching a-silicon layer is shown in fig 2(d). The SEM shows several micrometer long nanowires at the edge of a trench. The average width of the nanowires is 25 nm and spaced at around 22 nm. The uniformity in the height of the wires can be seen from the SEM of the cross-section of the template as shown in fig. 3(a). The flexibility of routing nanowires by PEDAL process is shown SEM image in fig. 3(b)

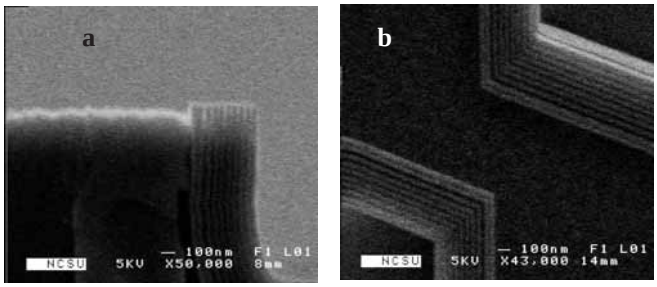

Figure 3: *SEM image* **(a)** Cross section of the nanowire template **(b)** Top view of the nanowire template.

5. CONCLUSION

The new PEDAL lift-off process is useful in wafer-scale fabrication of aligned nanowires directly on the wafer. Nanowire structures with 25 nm average width spaced at 22 nm have been demonstrated. PEDAL lift-off process has the potential to fabricate sub-10 nm nano-wires with 20 nm pitch using slower LPCVD process or the Atomic Layer Deposition process. The fabrication facilites required for the process are readily available. The PEDAL process can also be used to make templates for the wafer-scale nano-imprinting or for making nanowires of different metals directly onto wafer by metal evaporation followed by lift-off of the required metal. The process has the flexibility of routing the nanowires around the Logic and memory modules across the entire wafer without resorting to multiple alignments. For technological applications, it is necessary not only to have nanowires fabricated into highly ordered array with predetermined spacing and registry but also to know the location and registry between wires precisely for making contacts. The PEDAL process gives wires with precise beginning and ending location depending on the definition of edges of trench, allowing contacts to the wire to be made in predetermined manner.

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