A Unified Compact Model for Electrostatic Discharge Protection Device Simulation

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ABSTRACT

Snapback phenomenon plays an important role for electrostatic discharge (ESD) protection design, in particular for very large scale integration (VLSI) circuits. In this paper, we proposed a unified ESD model for metal-oxide-silicon field effect transistor (MOSFET) and silicon current rectify (SCR) devices. This new model characterizes the snapback characteristics and can be directly incorporated into ESD circuit simulation for whole chip ESD protection circuit design.

Keywords: compact model, ESD protection, circuit simulation, MOSFET, SCR, snapback, whole chip design

1 INTRODUCTION

In modern micro- and nano-electronics manufacturing, whole chip ESD protection circuit design is necessary for obtaining robust electrical performance [1-5]. In designing the whole chip ESD protection circuit, owing to the circuit complexity, an accurate and efficient computer-aided design (CAD) tool is not only helpful but also essential [5-10]. Several ESD models for MOSFET or SCR devices have been proposed [11-15]; unfortunately, they are constructed upon simplified bipolar junction transistor (BJT) models. Most of these BJT-based ESD models results from the fact that BJT models can only describe device behavior under the normally operation region. Therefore, they lack physical meaning in the ESD region and may trouble circuit design applications.

We propose here a unified ESD model for MOSFET and SCR devices, shown in Figs. 1-3, with a set of algebraic equations and limited parameters. Moreover, application of our recently developed automatic and intelligent parameter optimization technique, a series of comprehensive simulation is performed, which confirms the proposed model can be successfully applied on MOSFET and SCR devices for preliminary ESD simulation. This paper is organized as follows. In Sec. 2, we state the proposed ESD model. In Sec. 3, we show the results and compare with the measured data for MOSFET and SCR devices. Finally, we draw conclusions.

2 THE PROPOSED ESD MODEL

The developed ESD model is basically developed on the device physics that parasitic BJT will breakdown under the ESD stress. Figure 4 shows the characteristics of ESD considered in our model. According to the mechanism, we can simply formulate the snapback current - voltage (IV) characteristics by using a current controlled voltage source (the breakdown voltage of parasitic BJT) V_{BCE}, the series resistance caused by R_d and the external resistance R_x resulted from measurement instruments. The IV follows the equation (1). The current controlled voltage source V_{BCE} could be simply expressed by the following equation (2) where B can be obtained from Eq. (3), in which R and C can be simply solved from Eqs. (4) and (5).

$$I = \frac{V - V_{BCE}}{(R_x + R_d)} \tag{1}$$

$$V_{BCE} = V_{BCE0}(1 - B^{-1})^n \tag{2}$$

$$R(\frac{I}{B}) + \ln(\frac{I}{B}) + C = 0 \tag{3}$$

$$R = \frac{Z_s + r_e}{V_t * \alpha_b} \tag{4}$$

$$C = Z_s * \frac{I}{V_t} + \ln(I_s * \alpha_b) \tag{5}$$

There are six parameters have to be optimized in the equations above [16]; they are R_d, n, Z_s, r_e, I_s and α_b. In the model, R_x reflects the impedance of transmission line which equal to 50ohm, and V_t is the thermal voltage. The other parameters all have their physical meaning: n is the idea factor of pn diode, Z_s is the substrate resistance, r_e is emitter resistance, I_s is the revise saturation current, and the α_b is the common base current gain. Our model could be simply performed by considering the optimization of 6 parameters through the comparing between solved IV data to measured data. This approach enables the simulation of the whole chip ESD robustness.

3 RESULT AND DISCUSSIONS

We compare the modeled and the measured snapback characteristics of MOSFET device in Fig. 5 and SCR devices from the Figs. 6 to Fig. 10. It is clearly found that our model precisely describes the snapback behavior of both the MOSFET and SCR devices under ESD events.

Figure 5 compares the modeled and the measured snapback characteristics of the MOSFET device; it demonstrates that our model successfully achieves four major features. Those are trigger-on voltage, snapback slope, holding voltage and turn-on resistance. With correctly modeling those four characteristics, the designers could easily find out if the design margin is enough for avoiding both the ESD damage and latchup; moreover, the efficiency of both protection-activating and layout-drawing can be also optimized through the simulation.

Figures 6 to 10 presents the snap back IV characteristics of the SCR devices with different emitter to base spacing. It could be easily found that all the SCR devices have similar turn on voltage (~12V), but the holding voltages are different. The holding voltage will significantly increase with the decreasing of the emitter to base spacing. With an estimating, about 3 volt of holding voltage difference could be found. Modeling reflects the measurement results. It could be also found that a decreasing of emitter to base spacing will cause a higher holding voltage. This result is caused from the fact that the built-in potential between p-well and n-well is dominated by minority carriers which also influence on our model through the parameter n and αb. Make it more clearly that the higher minority carrier existing in the well region will cause a lower built-in potential; consequently, result in a lower holding voltage. Owing to a higher efficiency in sinking out the minority carrier, the SCR with the shorter emitter to base distance will certainly has a higher holding voltage. Finally, it is also noticeable that the jiggled IV curve is not the nature characteristics of device but caused from the fluctuation of data sampling.

Tables 1 and 2 illustrate the optimized parameters of all devices [16]. Among these results, we also evaluate the convergence property of the entire parameter range; after a comprehensive calculation, no singular point can be found. Moreover, it could be also drawn that every parameter set will converge at few inter-loops. Here, we can conclude that our model is a SPICE circuit simulation compatible result with no convergence difficulties.

4 CONCLUSIONS

In this paper, we have briefly presented an attractive unified ESD model for both MOSFET and SCR protection circuit design. The results have demonstrated good accuracy and high capability for both devices. We conclude that the developed ESD model could be performed in SPICE circuit simulator for desirable agreement with the measured ESD characteristics. Compared with conventional models, this model provides a novel way to ESD simulation and shows good computational efficiency.

5 ACKNOWLEDGMENTS

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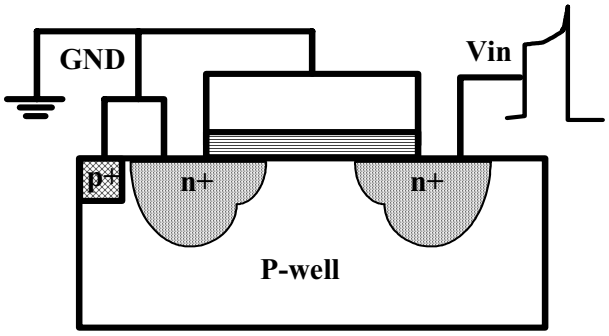

Figure 1: The device structure of the experimental MOSFET device.

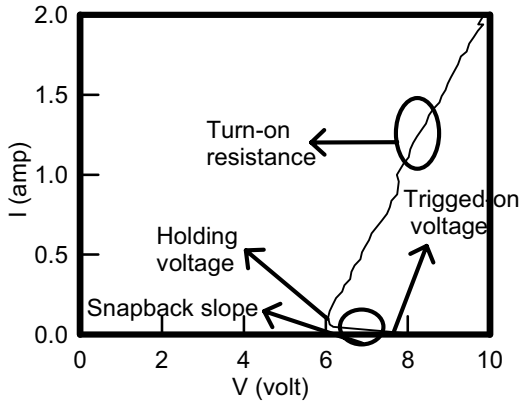

Figure 4: The characteristics of ESD considered in our model.

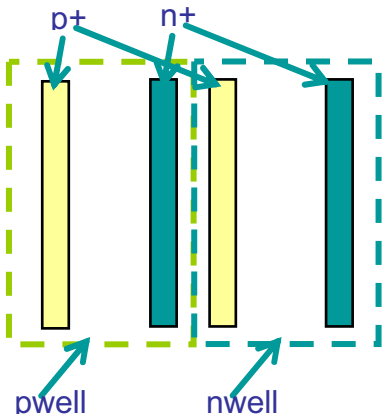

Figure 2: The top layout view of the investigated SCR device.

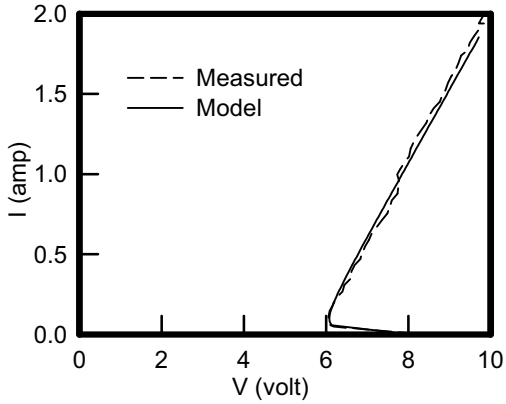

Figure 5: Comparison between the measurement and simulation of the MOSFET device.

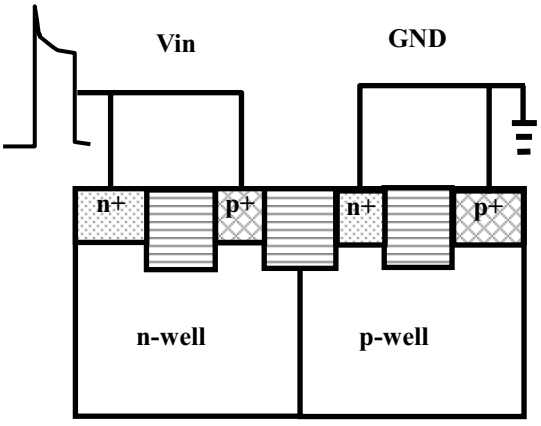

Figure 3: The device structure of the experimental SCR device.

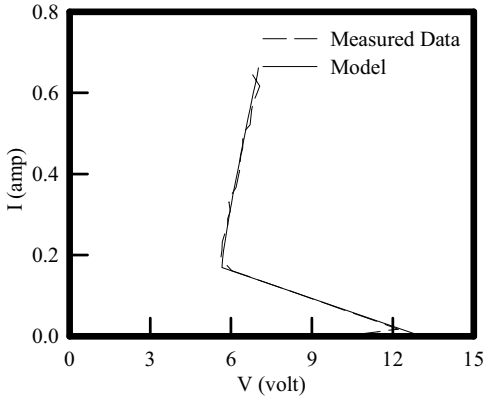

Figure 6: Comparison between the measurement and simulation of the 1μm SCR device.

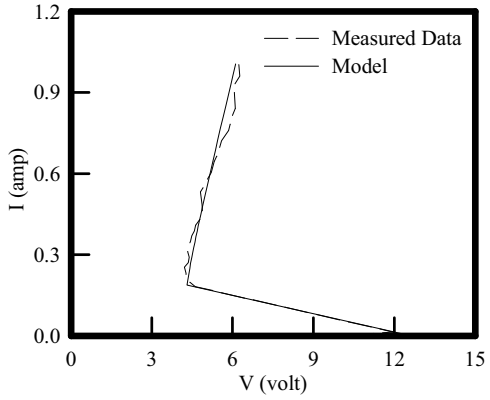

Figure 7: Comparison between the measurement and simulation of the 2μm SCR device.

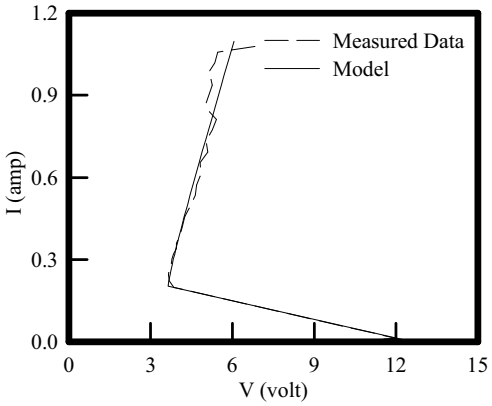

Figure 8: Comparison between the measurement and simulation of the 5μm SCR device.

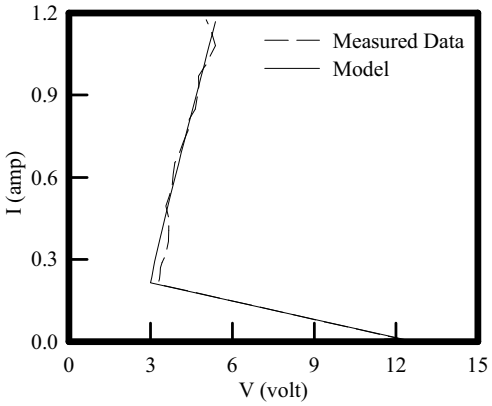

Figure 9: Comparison between the measurement and simulation of the 10μm SCR device.

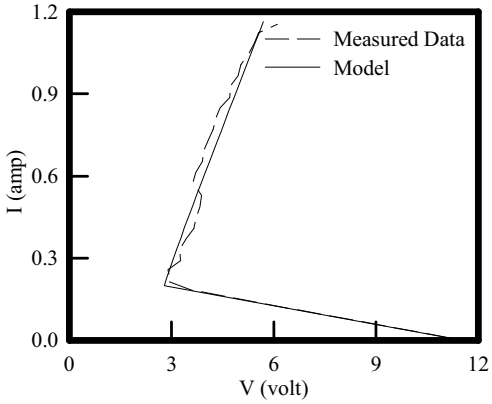

Figure 10: Comparison between the measurement and simulation of the 20μm SCR device.

Paramete	Unit	Value
R_d	ohm	2.5
V_{BCE0}	V	7.5
n	none	1
Z_s	ohm	100
R_e	ohm	5
α_b	none	0.9

Table 1. A set of the optimized parameters for MOSFET.

	Device Geometry				
Parameter	1μm	2μm	5μm	10μm	20μm
R_d	3.30	2.42	2.97	2.68	3.13
V_{BCE0}	13.08	12.59	13.08	13.08	11.49
n	2	1.65	2.09	2.23	2.05
Z_s	50	82.60	54	63.9	96.39
R_e	27	21.47	18.77	24.63	23.26
α_b	0.61	0.67	0.71	0.76	0.71

Table 2: A set of the optimized parameters for SCR with different dimensions.