A Novel Method of Fabricating Optical Gratings Using the One Step DRIE Process on SOI Wafers

A. Cooper*, P. T. Docker** and M. C. Ward***

* *Mircro and Nanotechnology Group, School of Engineering, Mechanical and Manufacturing Engineering, University of Birmingham, Edgbaston, Birmingham B15 2TT,*
Email: awc@bham.ac.uk , ** p.t.docker@bham.ac.uk , *** m.c.ward@bham.ac.uk

ABSTRACT

This paper describes a novel technique for manufacturing optical gratings using the one step DRIE (Deep Reactive Ion Etching) process. Utilising the notching effect documented in previous work when working with silicon on insulator (SOI) wafers, fully released, intact gratings have now been produced without the requirement for additional releasing processes. The one step process eliminates the possibility of stiction which can occur when "wet" processing chemistry is used in the release of microstructures. It should be noted that all DRIE etching in this work was performed using a Surface Technology Systems DRIE which uses a process developed from the Bosch process (R B Bosch Gmbh 1994 US Patent Specification 4855017 and German Patent Specification 4241045CI) termed 'time multiplexed deep etching' (TMDE) [1].

Keywords: gratings, notching, soi, dry-release, optical

1 INTRODUCTION

Deep reaction ion etching (DRIE) and silicon on insulator (SOI) wafers are well established technologies for the manufacture of released MEMS structures. These structures are normally released through the removal of the buried insulator layer, which is removed with an etchant [2]. Typically the etchant is then dispersed from the structure by rinsing with deionised (DI) water which is then dried through evaporation. Unfortunately the flexible microstructures can be pulled together or down onto the substrate at the last moment of drying by the capillary pressure induced by the droplet in the gap. These structures can remain stuck together even after completely dried, if the adhesion force between the contacted areas is larger than the elastic restoring force of the deformed structure. This phenomenon is more commonly called "stiction" in the field of microelectromechanical systems (MEMS).

When fabricating optical gratings, "stiction" is particularly undesirable because the beams of the gratings can stick to one another resulting in an imperfect grating.

In recent years, to try and eliminate the need for this wet processing, a number of workers [2-4] have developed a method of dry releasing microstructures on SOI wafers using DRIE. This method involves using the undercutting or notching phenomenon [5,6] that is observed when the buried oxide is exposed during the etching of high aspect ratio trenches.

Additional work was carried out by Docker *et al* [7] to further enhance this technology through the use of sacrificial 'waffle' type structures that allow large areas of silicon to be cleared from SOI wafers without the formation of silicon grass. These 'waffle' type structures were designed to simply float free from the surface of the SOI wafer when they had been under-etched and released. The waffles were originally used when etching device layers measuring 20 microns thick and failed catastrophically when they were released.

The new work demonstrates how modified waffle structures, when etched into a 300 micron device layer of a SOI wafer, can form intact released optical gratings. Unlike the standard waffle structures, these new gratings are made up of long trenches dimensionally wider by an order of magnitude. Their depth is also much greater than the standard waffle structures, measuring 300 microns as opposed to just 20 microns.

2 GRATING DEVELOPMENT

It is believed that the larger feature size of the gratings is the key feature responsible for the devices not being eradicated by the etching process. The height of the damage caused by the notching effect which releases the structures is limited, leaving the gratings with deep, parallel wall profiles. When released by the notching phenomenon, the gratings do not fail like the shallower waffles and they remain present on the wafer until it is removed from the etching chamber. The gratings can then be removed from the wafer by simply tipping the wafer through 180 degrees and letting the gratings fall onto a soft surface.

One of the key features in being able to etch the gratings to the 300 micron depth had been in the utilisation of a thermal oxide mask instead of the normal photo-resist mask for the etching process. This has enabled a very accurate feature size of the gratings to be maintained which would not have been possible using one very thick or multiple layers of photo resist.

The oxide mask is fabricated using conventional photolithography on top of the oxide layer which is then subjected to a plasma oxide etch to create the oxide mask. A one micron thick layer of oxide proved sufficient to withstand the DRIE process for the 130 minutes required to etch the 300 micron depth of the device layer and undercut the gratings allowing them to be released. The etch time required for release of the gratings was found simply by visual inspection.

3 FABRICATED GRATINGS

Figure 1 shows a grating with a 40 micron beam width and 40 micron spacing "in situ" on a 300 micron thick SOI wafer after etching.

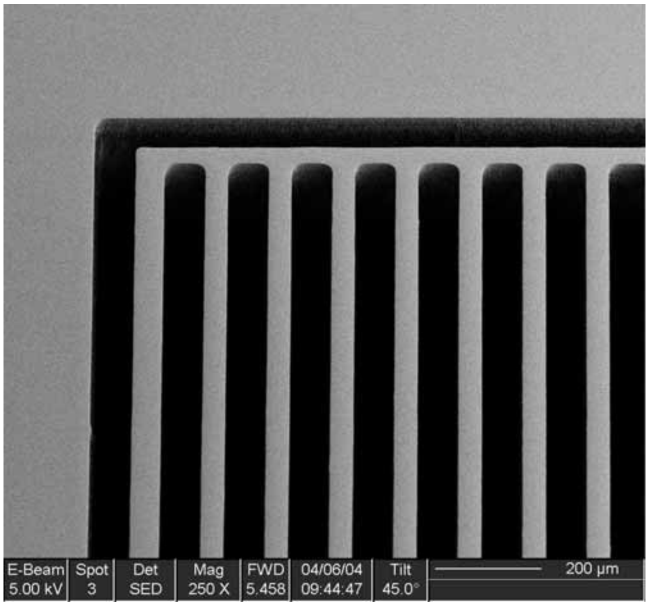

Figure 1: A grating "in-situ" on a SOI wafer after etching

Figure 2 shows the same grating after the under-etching process was completed and the grating was removed from the SOI wafer.

The photolithography performed to produce the gratings shown in figures 1 and 2 was done using acetate masks as opposed to conventional chrome on glass masks. This was done to reduce development costs due to the large number of grating masks that were needed for the project. For this reason the surface of the walls of the gratings is not as smooth as it is believed possible to achieve using conventional chrome on glass masks. This is due to the larger tolerance and minimum feature size that is a characteristic of the acetate masks.

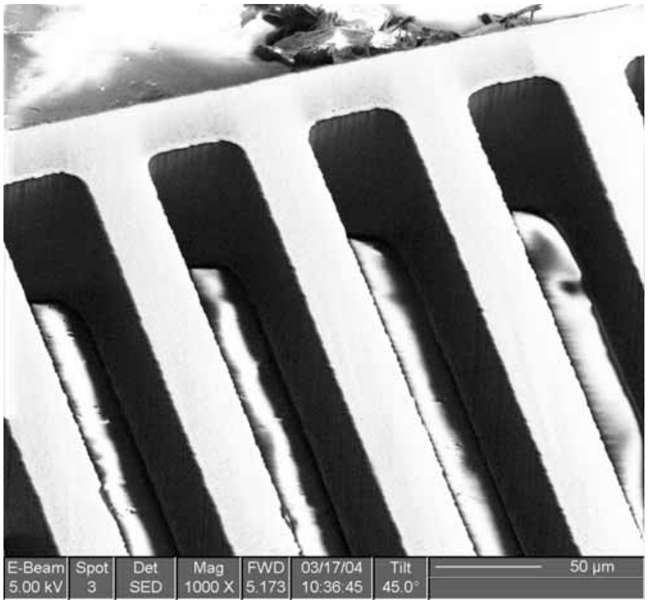

Figure 2: A grating removed intact from the SOI wafer

4 POTENTIAL APPLICATIONS FOR HIGH ASPECT RATIO GRATINGS

One of the most interesting features of the gratings is the high aspect ratio of the microstructures. With an aspect ratio of 7.5:1 the gratings lend themselves to the possibility of being used as optical switches that work by means of a tilting or rotating action. The gratings reported in this paper would require a tilting angle of only 7.6 degrees out of plane of the light source to stop light from passing through them.

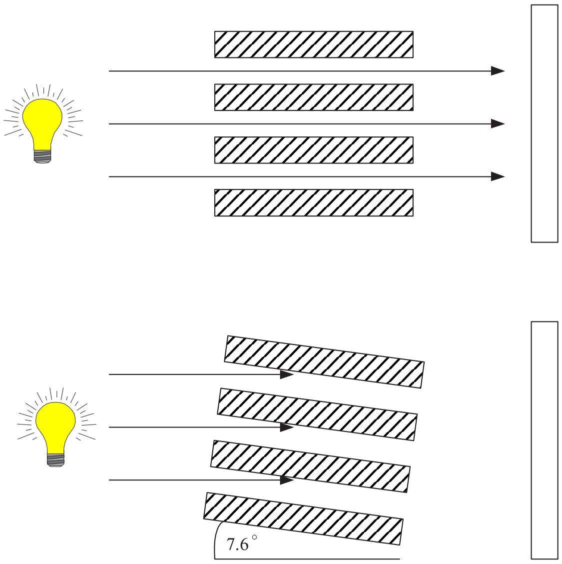

Figure 3: Schematic diagram of how the gratings might be used in switching applications

This is illustrated in figure 3 and it is believed that gratings with an aspect ratio of over 20:1 could be produced, reducing the tilting angle required to less than 3 degrees. In the field of microelectromechanical systems (MEMS) where the performance of devices such as switches is often governed by the displacement available from low voltage actuators, a device requiring such a small displacement could prove to be a valuable tool for use in optical switching technology

5 CONCLUSION

This paper describes a novel method of fabricating fully released optical gratings from SOI wafers using the one step DRIE process. Gratings with a 40 micron beam width and 40 micron gap width were fabricated from 300 micron thick device layer SOI wafers. The gratings were successfully dry released and removed from the wafer whilst maintaining their structural integrity.

The successful fabrication of these high aspect ratio gratings shows great promise for applications such as optical switching. The large aspect ratio of the grating means that they would only have to be tilted a few degrees out of plain with a light source to obstruct light from passing, effectively performing the role of an optical switch. These filters could prove to be a timely discovery with the current shift towards optical signal processing.

REFERENCES

[1] Bosch R B Gmbh 1994 US Patent Specification 48855017, and German patent Specification 4241045CI.

[2] Volland B E, Heerlein H, Kostic I and Rangelow I W, “The application of secondary effects in high aspect ratio dry etching for the fabrication of MEMS” Microelectron. Eng. 57-58, pp 641-650, 2001.

[3] Ayon A A, Ishihara K, Braff R A, Sawin H H and Schmidt M A, “Microfabrication and testing of suspended structures compatible with silicon on insulator technology” J. Vac. Sci. Technol. B 17, pp 339-349, 1999.

[4] Docker P T and Kinnell P K, “A dry single step process for the manufacture of released MEMS structures”, J. Micromech. Microeng. 13, pp790-794, 2003.

[5] McAuley S A, Asraf H, Atabo L, Chambers A, Hall S, Hopkins J and Nicolls G, “Silicon micromachining using a high density plasma source”, J. Phys. D: Appl. Phys. 34, pp2769-2774, 2001.

[6] Gormley C, Yallop K, Nevin W A, Bhardwaj J, Asraf H, Huggegett P and Blackstone S, “State of the art deep silicon anisotropic etching on SOI bonded substrates for dielectric isolation and MEMS applications”, Fifth Symp. Semiconductor Wafer Bonding Svience, Technology and Application, The Fall Meeting of Electrochemical Society (Hawaii, USA) Oct 17-22, 1999.

[7] Docker P T, Kinnell P K and Ward M C L, “Development of the one-step DRIE dry release process for unconstrained fabrication of released MEMS devices”, J. Micromech. Microeng. 14, pp941-944, 2004.