

Development of a Scaleable Interconnection Technology for Nano Packaging

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ABSTRACT:

Microelectronics miniaturization is following Moore's law since the mid sixties and over the years it has always been possible to follow it without meeting fundamental technological limits. This might be in question for future applications, where SIA roadmap shows a red brick wall for the further development of microelectronics without fundamentally new approaches. These new approaches as single atom and CNT based transistors do all target on maximum integration on chip level, leading to increased interconnect density and thus to a miniaturization of the individual contact. Parallel to the miniaturization of the interconnects the development of scaleable interconnect technology is necessary, providing reliable infrastructure for future packaging needs.

At Fraunhofer IZM various approaches towards a scaleable interconnect technology are researched. This paper will describe the development of reactive interconnects, i.e. contacts that need no external energy source, but release the energy for solder interconnect formation by exothermic reaction of a nano-enhanced encapsulant. Potential areas of application are interconnection of thermally sensitive devices as bio sensors or interconnection on low cost substrates, e.g. for the smart card applications or the expanding RF ID tag market. The current status of technological developments for the realization of reactive interconnects is described, including interconnect bumping, reactant application and interconnect formation. These technological processes are backed by thermal simulation. Summarized, this paper shows the potential of reactive interconnects being a "drop in" solution that not only allows the cost effective packaging of today's μ scale ICs but also tomorrows nano-scale devices.

1. Introduction

The consequences of downsizing in assembly and interconnection as well as in packaging technologies are twofold: on one side the I/O density on chips is increased, causing a lateral x-y reduction in pitch and pad size of the interconnections, the driving force here is the increase of functionality per area due to progress in chip fabrication. Size reduction in the third dimension, z, is a consequence of reduced overall system thickness after assembly: with chips 10-20 μm thick and substrates in the same range the gap between substrate and chip should be kept as small as possible, i.e. in a range well below 10 μm , reaching below the limits of today's $\mu\text{Packaging}$ into the nano range.

The shortest and thinnest interconnections between chips can be realized using flip chip technology. Here a chip is directly connected to the substrate by a solder bump. Depending on the technology pitches down to 40 μm (electroplating) and solder bumps with a height of 10 – 40 μm can be fabricated. For cost driven applications pitches of 80 μm are state of the art (stencil printing), bump height are around 30 to 40 μm [1]. Such solder bump heights result in a large gap between the chip and the substrate.

Considering the size reduction as well as the most cost effective process path the under bump metallization using the electroless deposition of Ni. Formation of solder caps by immersion solder bumping and subsequent interconnection by thermode bonding is a highly promising process chain for large scale low cost ultra-thin electronic systems leading the way towards pitches below 20 μm .

If this bumping process is combined with a low temperature melting solder, similar to woods metal, with a resulting melting point well below 100 $^{\circ}\text{C}$, low temperature joining becomes possible allowing the use of low cost flex substrates with glass temperatures just above 100 $^{\circ}\text{C}$. Typical joining process would be reflow soldering, that allows the use of existing equipment and of process know how.

To drive low temperature joining one step further it is possible to use reactive interconnects or reactive materials, resp., that provide a sufficient amount of energy at the solder bumps and allow solder melting and interconnect formation. This might not only be useful for the assembly on low cost substrate but can also be an interconnection technology for temperature sensitive ICs, e.g. biosensors or the like.

The experiments described are part of the feasibility investigations of low temperature joining and reactive interconnect processes.

IC preparation

For experiments 5x5 mm² dies with 45 μm diameter and 100 μm pitch with Al bond pads (Al_{0.7}Si_{0.5}Cu) and glass passivation over the active chip area.

Electroless Ni Deposition

After an initial wafer cleaning the electroless Ni deposition sequence starts with a zincation process of the Al. The surface is roughened (Al loss 200 -300 nm) and covered with Zn. Subsequently in the Ni bath zinc is exchanged by nickel. After the initial exchange Ni deposits through an autocatalytic process. Due to Ni-bath chemistry phosphorous is co-deposited along with the Ni. In the present case the phosphorous content is around 10 % by weight. The nickel thickness can be determined with an accuracy of 0.3 μm by adjusting the dwell time in the Ni bath. The Ni-surface is rough and exhibits spherical protrusions with heights in the range of 0.1 μm . The protrusions exceed this value if bath parameters are not appropriately adjusted. As a final step the Ni-surface is chemically coated with a 80 nm Au layer in order to prevent Ni oxidation.

Immersion Solder Bumping

Immersion solder bumping has turned out to give the highest yield solder temperatures at about 60 to 80 $^{\circ}\text{C}$ above the melting point of the respective solder [2, 3]. The liquid solder is capped with a thick layer of glycerol. A schematic graph of the soldering apparatus is depicted in Figure 1. Beside serving as a protection against contamination of the liquid solder it is used a heat reservoir to adjust the wafer temperature to the solder temperature. Glycerol also serves as a soft fluxing agent. Immersion speed into the solder is in the range of 3 to 10 mm/s. Hold time in the solder is 5 to 20 seconds. The pulling speed out of the solder is 10 to 20 mm/s.

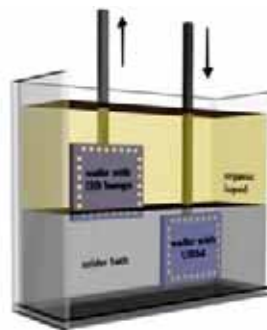


Figure 1: Schematic drawing of the immersion soldering.

The solder attaches to the wettable Ni (Au) surfaces on the and forms a cap shaped solder deposit. The outcome of the soldering process is investigated mainly by profilometer scanning, SEM cross sectioning. The morphology of the solder cap depends on the size and shape of the contact pad and also on the intermetallic phases that may be formed during the wetting process.

For chip bumping an InBiSn solder with a composition of In 51,0 - Bi 32,5 - Sn 16,5 wt%. This low temperature solder has a melting point T_m of 60,5 $^{\circ}\text{C}$, a density of 7,5

g/cm³ and a thermal conductivity of λ (@ 53 °C) of 17,8 W/m K. An example for such a solder bump is depicted in Figure 2, EDX-scans illustrate the composition of the major inter metallic compounds, the InBi-rich phase and the SnIn-rich phase

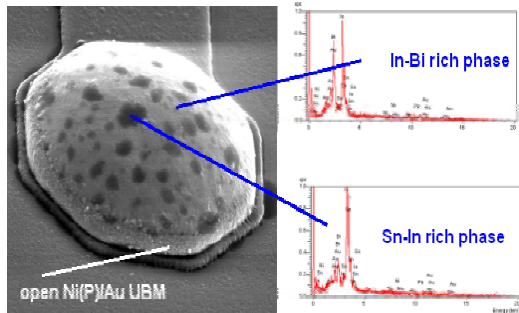


Figure 2: SEM micrograph of an immersion bump of InBiSn on a 40 µm Al pad

From related experiments, it was found that for solder caps in a profilometer scan line over 30 µm pitch solder bumps the variation in cap heights among caps is rather large, i.e. in the order of $\pm 30\%$. Moreover, outliers with solder caps much higher than average are found. The large spread in cap heights seems to be detrimental on first sight. However, in the subsequent thermode bonding process most of the solder will be squeezed from the middle to the edges of the contact pad until a homogeneous solder thickness between the contact pad is reached.

Thermode Bonding

For first experiments concerning the joining behavior a thermode bonding process joining chip on chip was used. Thermode bonding in itself is not a cheap process, however, high accuracy placement and the option to deliberately set force and temperature gradients during the bonding process is not possible with other techniques. In large scale production the cost can finally be reduced by appropriate process optimization.

The thermode bonding technology is based on very fast reflow soldering by pulse heating. We used the flip chip bonder FC150 from SUSS MicroTec. The fast process allows the use of low cost materials with low temperature resistance for flip chip soldering at high temperatures without damage of a flex or other sensitive materials. In our processes no underfiller was used, as focus was the determination of contact. A low temperature flux was used.

Examples and Reliability Results of Thermode Bonded Systems

During the immersion soldering process the Ni-UBM is exposed to the liquid solder for 30 to 60 seconds. For some investigated solder alloys a considerable formation of

intermetallics has been observed. Solders as SnPb, SnBi, InBiSn display only moderate intermetallics formation.

A typical cross section of an assembly at 100 µm pitch is shown in Figure 3. The left image shows a joint with optimum contact, while on the right side some oxide entrapment was visible. Reflow had taken place at 120 °C, under inert atmosphere. Joint thickness of these first samples is in the range of 20 µm including the Ni bumps. Figure 4 shows a row of solder interconnections generated by reflow with and additional scrubbing, i.e. a relative movement of the top IC versus the bottom one. This was introduced to minimize bond thickness and to get rid of the oxide entrapments.

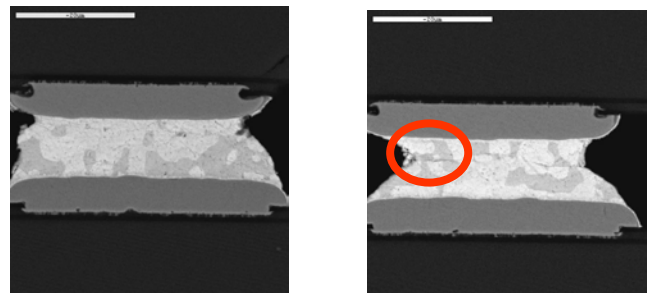


Figure 3: InBiSn ($T_m=62\text{ °C}$) placing and reflow at 120 °C. Close contact (l.) and contact with a thin oxide layer (r)

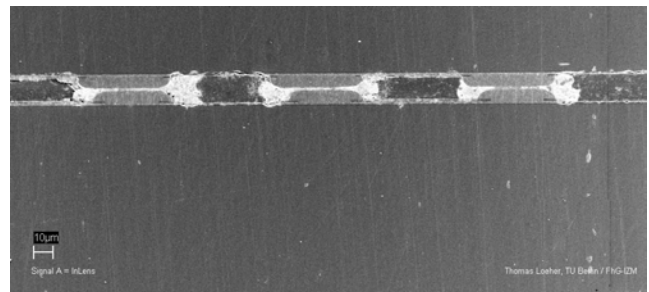


Figure 4: InBiSn ($T_m=62\text{ °C}$) interconnection with Ni(Au)-UBM pad size 45 µm, pitch 100 µm generated in scrubbing mode

These experiments showed that a successful formation of interconnects is possible with the low T_m solder. Further work was done to evaluate the potential of reactive systems to introduce the energy necessary for melting the solder.

Reactive System

To identify reactive material with the technical requirements:

- high thermal energy production in small space
- specific amount of heat
- controlled reaction rate
- spontaneous thus controlled ignition

- no or easy to clean reaction products

A potential system would most likely be a two component system, that reacts exothermically with low gas production. The system should have a low activation energy and should be moderate kinetically inhibited, to prevent overheating.

A first thermal simulation using a 2D model was performed to yield proof of concept. Boundary conditions were:

- No heat transfer to environment
- No melting energy
- Initial temperature is 25 °C (298 K)
- All Interconnects show ideal thermal conductivity

Aim was to vary bump and chip temperature for different amounts of energy. With the boundary conditions depicted in Figure 5, it was determined, that a short heat pulse of 100 ms with an energy of 5 mJ should be sufficient for solder melting and interconnect formation.

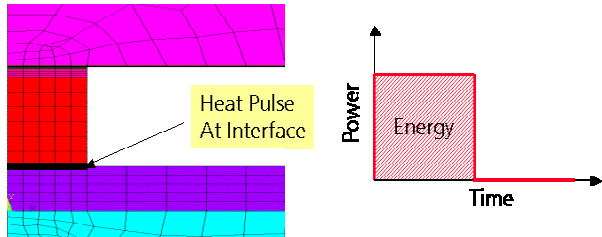


Figure 5: Boundary conditions of 2D thermal modeling. With the results of thermal simulation a market research was done and a system was identified, that matched the demands and was available for evaluation. This system consisted of commercially available substances, cyanate and amine, that allowed easy handling of liquid monomers and that showed quick polymerization after mixing. A highly exothermal reaction enthalpy was found with the system.

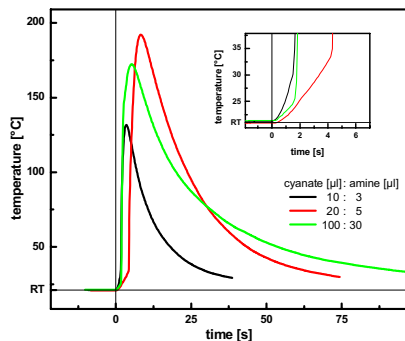


Figure 6:
Temperature pattern during polymerization

First soldering evaluation was performed with this system and it was found that solder bumps could be remolten using this reactive system. To this purpose a mixture of component A and component B was created by jetting the components on a solder depot. After an autocatalytic phase of 1 to 5 s within 1 s peak temperatures between 120 °C and 190 °C are reached

(Figure 6), where it is assumed that T-variations are due to the complex reaction mechanism. Nevertheless, solder T_m is reached in any case, the temperatures are reached for mixing ratios of 2:1 to 6:1 (cyanate:amine) and a total volume of 12,5 μ l to 130 μ l. Future work will deal with the transfer of this first laboratory results to actual test assemblies to evaluate the reliability potential of the process and technology.

Conclusions

We have shown that a combination of electroless Ni(P) UBM, immersion solder bumping and thermode bonding using a low temperature solder is a potential alternative for the assembly on temperature sensitive substrates or on temperature sensitive devices as biosensors. Additionally a feasibility evaluation of reactive interconnect technology has been performed that yielded promising results. We see this technology as one building block of packaging technology for miniaturized systems developing from a micro to nano scale. A large contribution of micro and nano technology is seen for the further evolution of packaging technology; actually, most of the obstacles predicted by state-of-the-art roadmaps for packaging technology can only be solved using nano technological means. Amongst all semiconductor-based research, the important contribution of packaging to a successful system in package realization should not be underestimated.

References

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