Application of Encapsulated PECVD-grown Carbon Nano-Structure Field-Emission Devices in Nanolithography

J. Koohsorkhi*, Y. Adbi*, S. Mohajerzadeh*, J. Derakhshandeh*, H. Hoseinzadegan*, A. Khakifirooz* and M.D. Robertson**

*Thin Film Laboratory,
Department of Electrical and Computer Engineering,
University of Tehran, Tehran, Iran, smohajer@tfl.ir
**Department of Physics,
Acadia University, Nova-Scotia, Canada, michael.robertson@acadiau.ca

ABSTRACT

A novel technique for submicron and nanolithography using vertically grown nickel seeded carbon nano-structures (CNS) on silicon substrates is reported. The field emission characteristic of carbon tips encapsulated in a titanium-dioxide insulator is utilized to create the nano-scale features. The electrical behavior of nano-structures indicates a precise control of the emission current with the surrounding gate electrode. Also by applying 100V between the cathode and resist-coated anode, lines with widths between 100 and 200nm have been drawn.

Keywords: carbon nano-tubes, nano-lithography, PECVD, vertical growth, encapsulation

1 INTRODUCTION

Carbon nanotubes and carbon nano-structures have drawn significant attention due to their various potential applications as high performance electronic devices, field emission displays, sensors and memory storage[1-2]. In particular vertically grown nano-fibers are of great importance in emission-based devices where nano-size tips are utilized to generate and control the emission current from tip towards the anode[3]. Several methods are being used to realize carbon nanotubes and nanofibers among which plasma-enhanced chemical vapor deposition is a well-established technique [4]. In this paper we report a novel self-defined PECVD-growth technique which employs the encapsulation of nano-tubes and allows formation of an electron-beam. The emission of electrons from the encapsulated tips is then exploited to perform low energy electron-based lithography. The structure proposed in this paper allows fabrication of field emission displays with a proper control on the emission level with the aids of an integrated gate electrode. Since a self-defined structure is used there is no need to lithography for the alignment of the gate with the central nano-tube. Using this approach, lines as thin as 100nm have been obtained although smaller features are expected. The electrical as well as physical characteristics of the grown structures have been investigated.

2 EXPERIMENTAL

Fig.1 shows the operation of the device where the electron beam is generated by the encapsulated carbon tips with a self-defined integrated electrostatic lens. The grown carbon-based nanostructures are responsible for electron emission and the surrounding metal, separated from the inner CNS by an insulating dielectric layer, acts as a self-defined gate to control the level of electron emission as well as a tool for beam shaping and focusing.

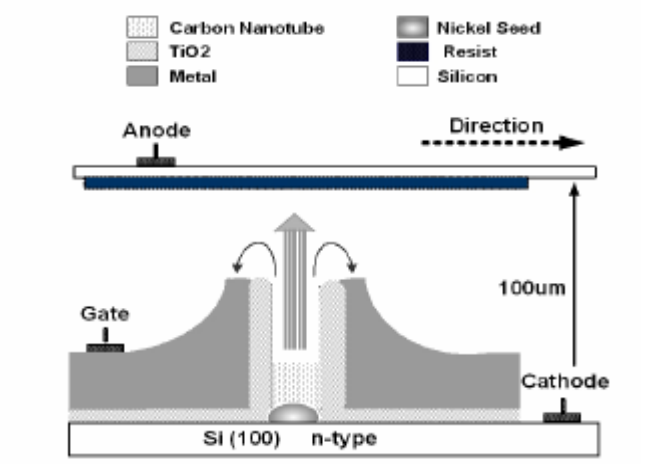

Figure 1: The schematic setup for the nano and submicron lithography using carbon nano-tubes.

The first step in the fabrication process is e-beam evaporation of a 5nm thick layer of nickel on (100) silicon substrates. The Ni-coated samples are then patterned using standard photo-lithography and are placed in a DC-PECVD chamber to perform the CNT growth. The pre-growth treatment is done at a pressure of 1.6torr in the presence of H_2 and at 650°C. After 15mins of H_2 blow, plasma turns on with a current of 30mA to form nano-islands with a typical size of 10 to 50nm. Immediately after, acetylene (C_2H_2) is introduced into the chamber to initiate the growth at a

pressure of 1.8torr. Fig.2 shows an SEM image of vertical CNTs grown with a high plasma density, indicating a near-vertical growth geometry.

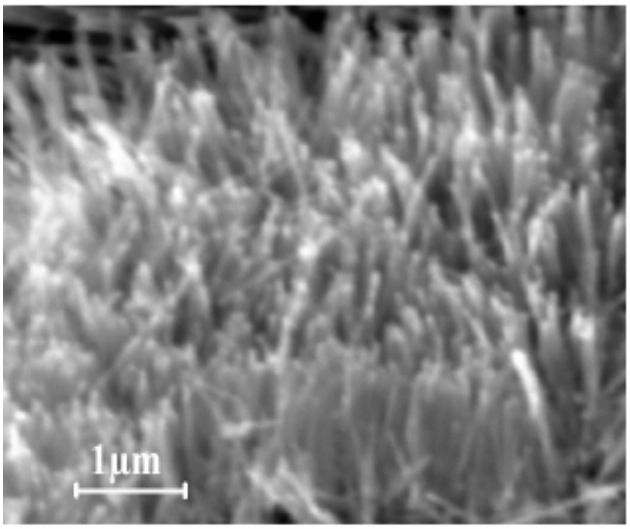

Figure 2: A close to vertical growth of CNT's on silicon substrates using the PECVD apparatus.

Fig.3 depicts the growth of conical nano-structures, achieved by varying the substrate temperature during the growth. The inset in this figure shows the sparsely distributed island growth, resulted from a reduced nickel thickness providing a structure suitable for nano-lithography applications.

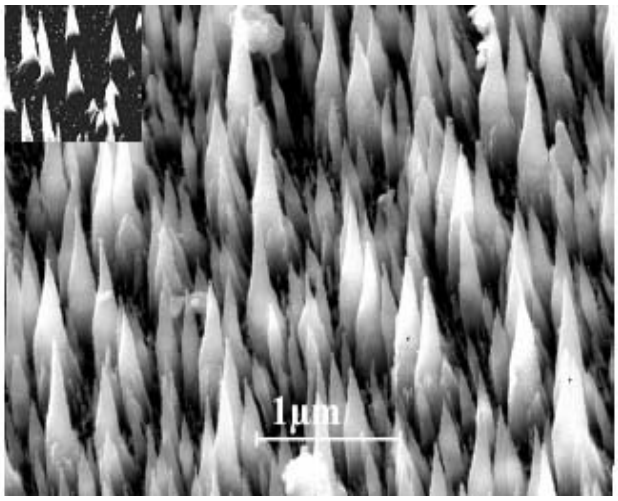

Figure 3: Growth of conical CNSs on Si substrate. Inset displays the sparse distribution of CNSs.

After unloading the samples, they are coated with 200nm of titanium-oxide using an atmospheric pressure CVD reactor at 220°C. The gate electrode is composed of 0.1μm-thick layer of Cr (or Ag) deposited by e-beam evaporation at 350°C. Final fabrication of the device requires one step of chemical mechanical polishing followed by plasma ashing to open up the nano-tips and to form partially hollow nano-pipes. This step is crucial in obtaining electron emission with a reproducible beam-shape and it is typically achieved by oxygen plasma ashing. Fig.4 shows an SEM image of a completed cluster of CNS's where all the fabrication steps were accomplished. The inset in this figure shows the magnified view of the completed nano-tips.

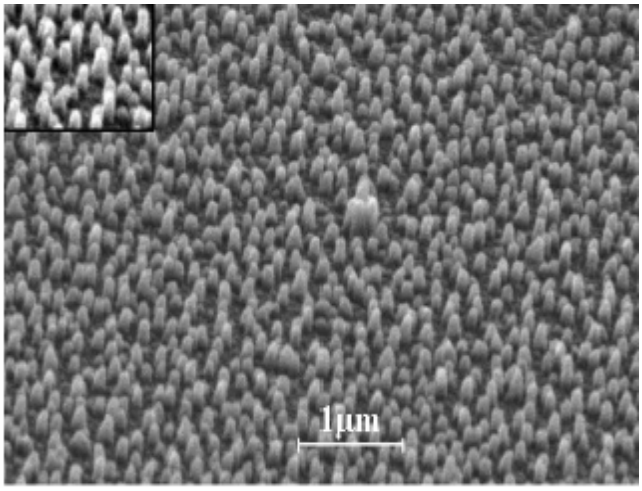

Figure 4: Final nano-tubes with metal and dielectric coatings. Photolithography of nickel seed layer can be used to form individual tips in desired locations.

Fig.5 depicts the electron emission current, measured at anode side against the gate voltage. As can be seen in this figure, increasing the gate voltage causes the emission current to drop significantly. The inset in this figure depicts the emission current in a semi-log scale. At a gate voltage of 10V, the emitted current begins to drop by more than three orders of magnitude.

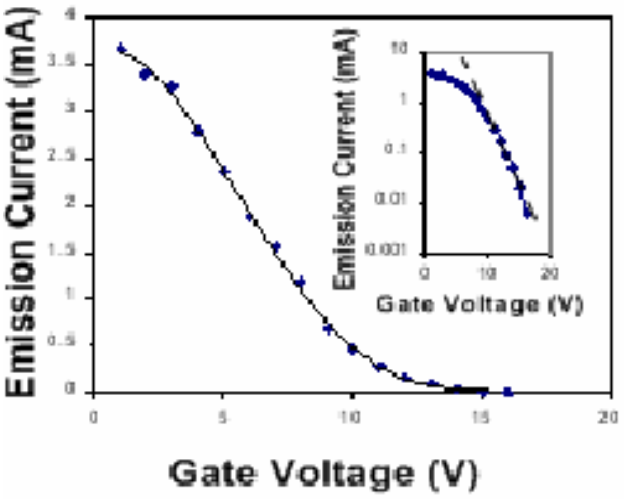

Figure 5: Emission current versus gate voltage. Inset shows the same results in a semi-log scale indicating the proper control of the gate on the emission current.

The effect of anode voltage on the current is also plotted in Fig.6 evidencing an almost linear variation of the current with respect to the anode-cathode voltage. As observed from Fig.5 and 6, the level of emission current is mainly controlled by the surrounding gate with less dependence on the anode voltage. At anode voltages below 50V, the emission current is almost constant and it is controlled mainly with the gate voltage.

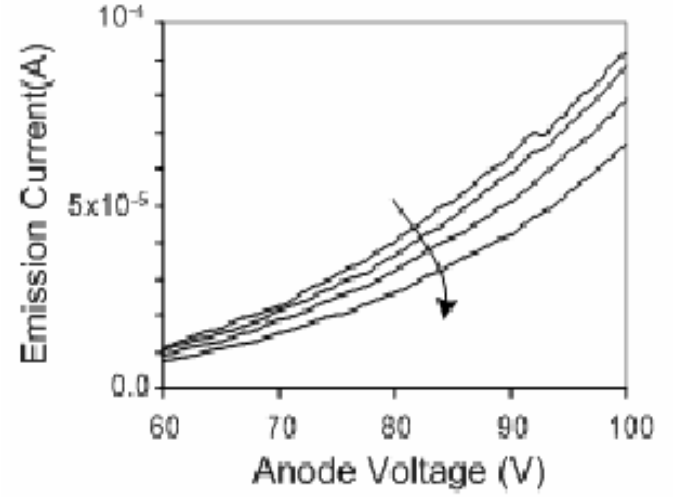

Figure 6: The Effect of anode voltage on the emission current. The arrow in this figure shows the effect of gate voltage.

By applying a proper voltage between carbon-tip and resist-coated substrate, electrons emit from the negative side onto the positive one and nano-size features are emerged. In this experiment we have used standard photo-resist.

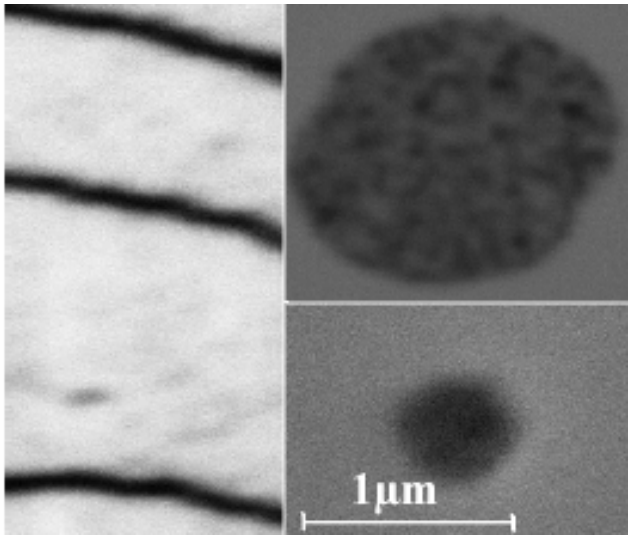

Figure 7: Evolution of nano-metric and submicron features by scanning the carbon emitter onto the surface of the top substrate using mechanical manipulation.

Using this technique, we have drawn lines with a width of 120nm and a length of 5 to 10µm. Also round dots smaller than 0.4µm were realized as shown in Fig. 7. The images at the right side of Fig.7 correspond to spots generated by holding the resist-coated substrate opposite to the electron emitting surface. The single spot at the bottom has a diameter of 400nm, whereas the top image belongs to the case where a cluster of nano-tubes have bombarded the resist-coated substrate.

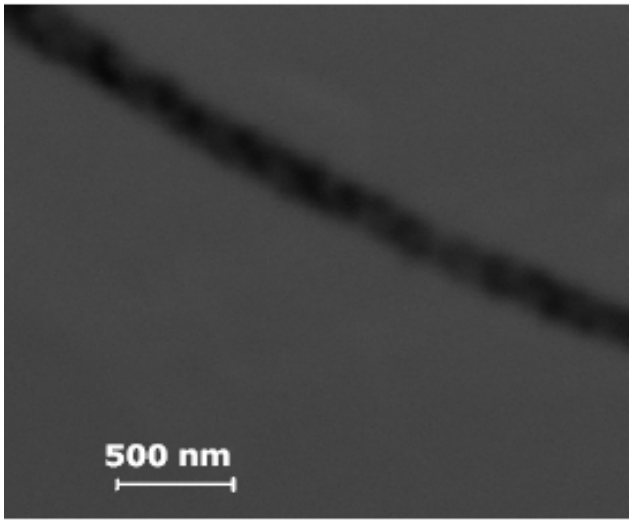

Figure 8: Submicron lithography with scanning the surface of the sample.

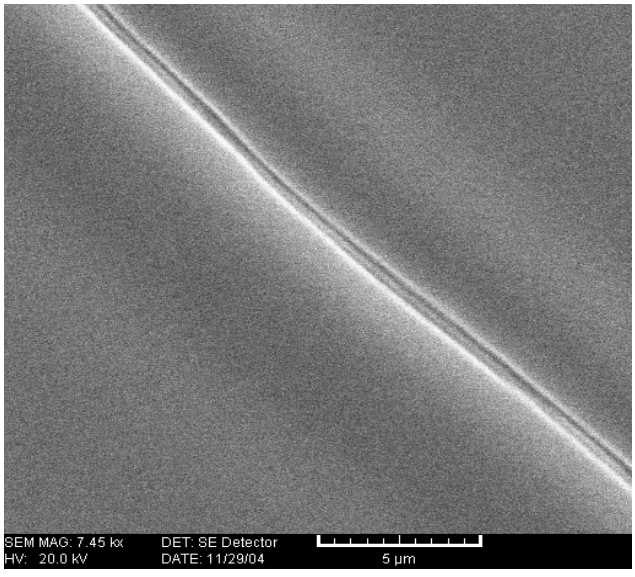

Figure 9: Straight lines with a length of 500um have been drawn using mechanical manipulation of nano-tubes.

Straight lines with thicknesses around 200nm have also been achieved (Fig.8 and 9). Also as seen from Fig.9, long lines can be realized using this approach which could be used for nano-wires. The width of the features depends

mostly on the diameter and shape of the grown CNS's. By extending this approach, we have been able to draw lines with a thickness of 48nm using conventional photoresists. Further reduction of the size of the lines and better mechanical manipulation of the tips are being pursued. We are also trying to realize deep sub-micron MOSFET devices using this nano-lithography technique.

3 ACKNOWLEDGEMENT

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