Fabrication of Well-aligned and Mono-modal Germanium Dots on the Silicon Substrate with Trench-ridge Nano-structures

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We perform the ability to fabricate germanium (Ge) dots on the silicon substrate with trench-ridge nano-structures by integrating electron beam lithography system (E-beam), reactive ion etching (RIE), and ultra-high-vacuum chemical vapor deposition (UHV-CVD). Two experiments are shown, and a model is hypothetically set up based on our analysis according to the statistics of dots. Most importantly, well-aligned and mono-modal dots are realized successfully by manufacturing about 30nm-width trenches, and we have the suggestion strongly that it is achieved by exploiting the high surface mechanical energy of ridge edges.

Keywords: Ge dots, aligning, nano-structures, E-beam

1 INTRODUCTION

Semiconductor dots are interesting systems because of their potential applications in novel devices. Among them, germanium (Ge) dots on silicon system have been extremely studied recently. The Stranski–Krastanow growth method is usually used to obtain silicon substrates. After the wetting layer deposition, Ge dots are formed spontaneously to release misfit strain. Generally, these dots nucleate at random positions and exhibit rather large size dispersions. In Ge dots on silicon system for growth temperature around 600 °C, typically a bimodal distribution is found, including pyramid- and dome-shaped dots [1]. However, the size and position distribution of these dots is critical to their application in novel devices [2]. How to control the spatial distribution and uniformity of self-assembled dots consequently becomes an essential issue.

Some ideas have been addressed to improve the spatial aligning and the uniformity of Ge dots [3, 4]. Recently, major progress was reported by integrating lithography and self-assembly techniques for ordering of Ge dots on silicon substrates [5, 6]. We perform to fabricate Ge dots on the silicon substrates with trench-ridge nano-structures. Most surprisingly, well-aligned and mono-modal Ge dots are realized by 30nm-width trenches. Comparison with published papers, the ordering dots we proposed are grown on the silicon ridges (the area not exposed in lithography process) instead of grown in the trenches, pits, or holes (the area exposed in lithography process) [5-8]. This point is never discussed, emphasized or realized in previous published papers.

The whole process is briefly stated as below. At first, it is started with E-beam (ELS-7500EX) to make nano-patterns on the substrates. Next, RIE is exploited for trench-fabrication. After etching, the resist is removed. Subsequently, a wetting layer is deposited and Ge dots are grown by UHV-CVD (SIRIUS CVD 400). Finally, the surface morphology is investigated in air with atomic force microscope (AFM).

2 EXPERIMENTS

Two experiments have been shown. In the first experiment, Ge dots, as Fig. 1 shows its atomic force microscopy (AFM) images, are grown on the 100nm-100nm, 200nm-200nm, 300nm-300nm and 400nm-400nm trench-ridge nano-structures. Each patterned area consists of trenches with 50nm depth. 20nm silicon is deposited as wetting layer. Subsequently, 7 equivalent-monolayers (eq-MLs) Ge is deposited on the prepatterned silicon substrate at about 600 °C. It is found that Ge dots are grown easier in the trenches than on the ridges, as Fig. 1 shows, for there are more dots appeared in the trenches than on the ridges. The sample with 400nm-400nm trench-ridge nano-structures is observed that Ge dots are both grown in the trenches and on the ridges. The others are observed that Ge dots are grown almost in the trenches.

In the second experiment, 30nm-70nm, 30nm-120nm, and 30-170nm trench-ridge nano-structures are fabricated under the same process described in the first experiment. The depth of trenches is also 50nm depth. A 20nm silicon layer is deposited on the prepatterned areas following by a 10 nm SiGe layer with Ge content =20%. Subsequently, 7 eq-MLs Ge are deposited at 600 °C. Fig. 2 shows the AFM pictures of these three samples and the sample with dots grown on no-patterned area. From Fig. 2, dots are only grown on the ridges. It is never seen in published papers. In other words, nano-trenches are used to confine the position of Ge dots and make it grow well.

3 DISSCUSSION AND MODEL

An important result is that Ge dots grown on the prepatterned substrate are mono-modal. For the growth temperature around 600 °C, a bimodal distribution is found, including pyramid- and dome-shaped dots, in the Ge dots on silicon system. From the AFM data, the statistics of Ge-dots diameter and height are gathered. It is observed that the diameter-to-height ratio (D/h) of pyramid-shaped dots is about 10, and the D/h of dome-shaped dots is about 5. We classify Ge dots according to D/h. Fig. 3(a)-(c) show the percentage of Ge-dots D/h, which compare the area without nano-structures and the one with 400nm-400nm trench-ridge nano-structures. It is noticed that the dots grown on prepatterned area, compared to the ones grown on no-patterned area, have the bimodal tendency, both on the ridges and in the trenches. Fig. 3(d) and (e) show the percentage of Ge-dots D/h, which compare the area without nano-structures and the one with 30nm-120nm trench-ridge nano-structures. Obviously, the Ge dots are mostly pyramid-shape, for D/h is mostly about 10. The mono-modal inclination of Ge dots on 30nm-120nm trench-ridge nano-structures is much more conspicuous than the ones on no-patterned substrate. Thus, we conclude that the dots grown in prepatterned area are uniform than those in no-patterned area.

We also consider the relationship between the morphology of structures and the dots distribution. Fig. 4(a) demonstrates 400nm-400nm trench-ridge nano-structures morphology versus Ge distribution, for x-axis represents the 400nm-400nm trench-ridge nano-structure, and y-axis represents the percentage of Ge distribution, which is taken the volume into account. The figure shows that Ge is not appeared at the edge of the ridge but tends to congregate at the corner of the trench. According to this observation, a model is hypothetically set up, which is used to conceptually explain the position of Ge quantum dots grown on the silicon substrate with nano-structures. We define a parameter *surface mechanical potential energy* (E_{smp}), which strain and structure curvature is attributed to it and determines the position of the Ge-dots growth. Under our definition, dots are preferentially grown in the lower E_{smp} area and unlikely to form in the higher E_{smp} area. Fig. 4(b) illustrates our idea that how the nano-structures morphology affects E_{smp}. It is expected that Ge is preferred to form dots in low E_{smp} area than in high E_{smp} one, and the Fig. 4(a) shows that Ge are not appeared at the edge of the ridge but tends to congregate at the corner of the trench. Thus, we deduce that the ridge edge is the high E_{smp} area while the trench corner is the low E_{smp} one, as shown in Fig. 4(b). Based on the thoughts, we plot morphology versus E_{smp} for the sample with 30nm-120nm trench-ridge nano-structures, as shown in Fig. 5. Because of the width of the trenches reducing to 30nm and the narrowness between two ridge edges, the E_{smp} of the trench corners is higher than that of ridge center. This is why the Ge quantum dots are formed on the ridges instead of being grown in the trenches. In other words, we make use of the ridge-edge strain to restrain dots from being grown in the trenches and align them well. Furthermore, modulation of the 30nm trenches can be used to control the spatial position of dots.

4 CONCLUSIONS

We fabricate Ge dots on silicon substrate with nano-structures. A model is hypothetically set up to explain the phenomenon according to Ge-dots statistics. Moreover, we exploit nano-trenches to align Ge dots. We claim strongly that dots can not be grown in the 30nm-trench area due to the high E_{smp} of the ridge edge. Under this technique, fabrication of well-aligned and mono-modal Ge dots on the silicon substrate with nano-trenches is successfully realized. It offers the potential applications of array for the implementation of nano-devices.

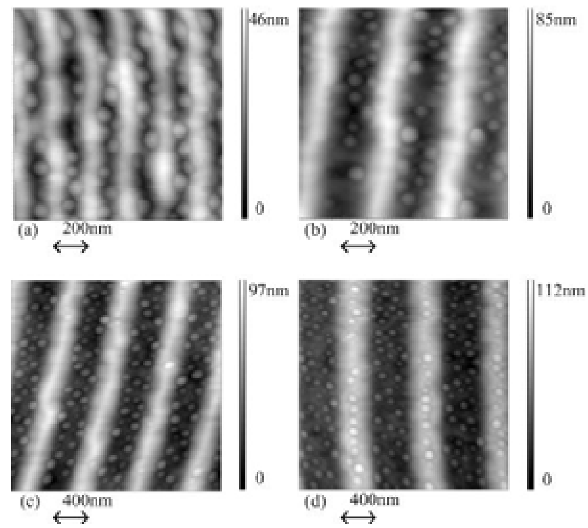

Fig. 1: AFM graphs of Ge quantum dots on the silicon substrate with (a) 100nm-100nm, (b) 200nm-200nm, (c) 300nm-300nm and (d) 400nm-400nm trench-ridge nano-structures

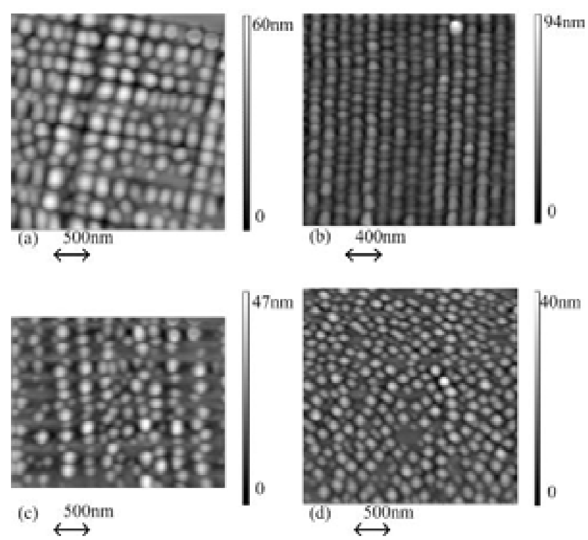

Fig. 2: AFM graphs of Ge quantum dots on the silicon substrate with (a) 30nm-70nm, (b) 30nm-120nm, (c) 30nm-170nm, and (d) no nano-structures

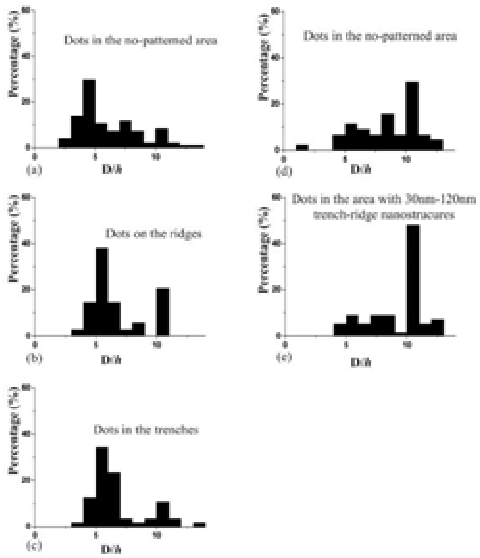

Fig. 3: the diagram of Ge-dots D/*h* percentage, which (a), (b), and (c) show respectively the area without nano-structures, the one with 400nm ridge, and the one with 400nm trench in the first experiment, and (d) and (e) show respectively the area without nano-structures and the one with 30nm-120nm trench-ridge nano-structures.

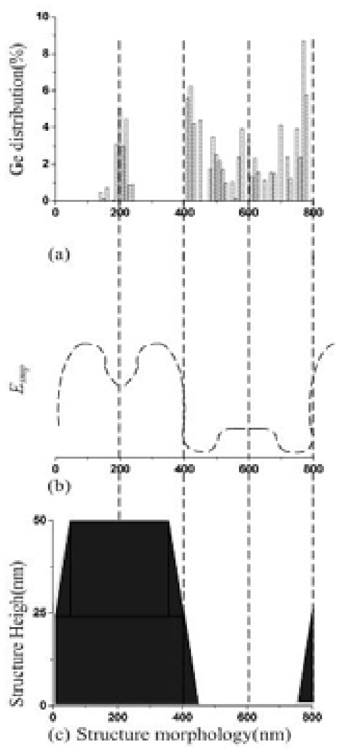

Fig. 4: (a) the percentage of Ge distribution, (b) the E_{smp} (hypothesized), and (c) the morphology versus 400nm-400nm trench-ridge nano-structures.

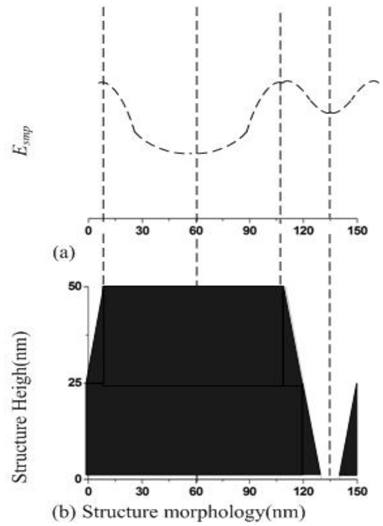

Fig. 5: (a) the E_{smp} (we hypothesize), and (b) the morphology versus 30nm-120nm trench-ridge nano-structures

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