A Gate Layout Technique for Area Reduction in Nano-Wire Circuit Design

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Abstract

This paper presents an homogeneous (array-based) approach for designing and manufacturing digital circuits using nano-tubes/nano-wires. As "a strategy for developing integrated devices with many individual elements has yet to be formulated" [1], it is evident that such an environment is a necessity for designing circuits using nano-wires. At logic level a novel formulation for area reduction is proposed and solved in polynomial time using a heuristic technique. The objective is to provide a further insight on the applicability of Moore's law to nanotechnology by evaluating the effects of area on logic design.

Keywords: Nano-wire, Nanotube, Circuit Design, Layout Optimization, Physical Area

1 Introduction

The feature size of basic devices (such as transistors) has constantly been decreasing over the past years. Today, transistors with gate lengths below 50nm can be fabricated and exhibit excellent electrical characteristics [2]. This trend has resulted in an almost exponential growth in integration level of electronic chips and integrated circuits, often referred to as Moore's law [3]. The architectural, and fundamental limits to this growth have been revised several times to account for new technologies; novel technological concepts (based on nano-devices and nano-electronics) are projected to be of primary importance [4] [5] [6] for future systems. Moreover, it is expected that so-called emerging technologies will not be limited by the fundamental barriers which are encountered today in for VLSI.

While fabrication of nano-devices presents considerable challenges, the high-level architectural organization at both device and circuit levels must be addressed. The unprecedented density and integration of these circuits necessitate novel arrangements for connections among nano-devices as well as input/output (I/O) of the chip; new techniques for handling a large number of connections (inclusive of electrical wires) are required to avoid undue heating, interference or "cross-talk" among them and exhibit proper control [7].

This paper presents novel techniques; a homogeneous array based methodology for nano-circuit implementation using nano-wires (e.g. carbon nanotubes) is presented. Initially, a circuit is represented using a set of standard Sum of Products (SoP). A minimal set of the products is constructed to cover all SoPs using a 2-level logic optimizer. The homogeneous array is then constructed by mapping each product term to a nano-wire. A nano-wire implements and connects multiple nano-devices to reduce the number of required contacts. A placement of the contacts for driving the inputs to the array and nano-devices is then formulated as a combinatorial Traveling-Salesman Problem (TSP). This instance is solved using the Lin-Kernighan heuristic to establish the placement of the nano-devices and their gate contacts, thus achieving a substantial saving in the physical layout for masking. This is required due to the difference in size between a nano-device metal gate and the nano-wire in its implementation.

2 SoP Based Array Design

Using nanotechnology, the active elements of a circuit (e.g. its transistors) can be made very small; however, the information transfer among these elements and the extraction of output/input signals from the circuit present difficult challenges due to the physical limitation of the contacts, i.e. the size of a contact is relatively large compared to a nano-device, thus often degrading the area benefits associated with a nano-scaled layout. An intra-molecular circuit implementation provides a promising design alternative; simple INV and NOR2 circuits have been proposed in [8] [9].

These techniques can be extended to circuits by utilizing basic boolean transformations, such as Sum of Products (SoP). For a SOP, each product term is mapped to a single nano-wire and implemented in a fashion that is reminiscent of Pass-Transistor logic design, as commonly encountered in CMOS. In this arrangement, one end of the nano-wire is constantly driven to logic 1 (high), while the other end represents the logic value of the product term. Nano-devices (as transistors) are placed along the nano-wire, Figure 1 shows a product term of 3 nano-devices.

Multiple nano-wires (each implementing a product

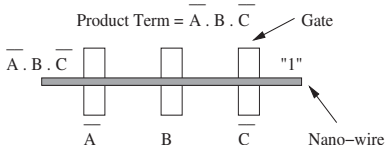

Figure 1: Nano-wire for constructing a product term

term) can be assembled into a nano-circuit; the gate of a nano-device occupies a rectangular area of metal placed over a nano-wire to form a nano-device, similar to traditional CMOS technology, i.e. a polysilicon crossing over an active diffusion area makes a MOS device. The metal gates are arranged in an homogeneous pattern to build the product terms and implement the nano-circuit. The important benefit of this approach is that *the nano-circuit design is effectively accomplished by a conventional process*, because patterning and etching of metal gates already use this technology. In this case the requirements are as follows: 1) the nano-wire must act in a fashion similar to a depletion mode MOS device, i.e. conducting with no field effect and semi-conducting in the presence of the field effect; 2) the on-resistance must be low, so many nano-devices can be connected in series with little effect on logic levels; 3) the threshold voltage must be low, thus allowing non-complementary operation in the nano-devices. This approach is different from [8] [9], because in the proposed design, the behavior is not complementary and complex (top) gates can be generated at relative ease (as multiple nano-devices can be placed along the same nano-wire).

The proposed approach offers substantial benefits because the source-drain contacts of the device are effectively removed (because the nano-wire acts as contacts between the source and drain of the nano-devices) and there is little added complexity in pattern-based processing steps for the nano-wires at manufacturing (in particular there is no need for complex patterning as in the active diffusion areas of conventional CMOS processes). Moreover, the *Schottky* barrier effect ([10]) is considerably reduced (i.e. it is distributed among multiple nano-devices).

2.1 Sizing

A problem which is commonly encountered in the layout for physical design, is size matching because even *the smallest feature sizes available today are substantially larger than a nano-wire diameter* (e.g. 130nm feature size and a 1.5nm wide nano-wire), thus degrading the possible benefit in area (and ultimately density) due to the small size of the nano-wires. Figure 2 shows two horizontally aligned nano-wires, the vertical adjacency between gates causes them to be spaced further away, thus adding to the unutilized (wasted) area. However this arrangement can be also viewed in a diagonal direction. In this case, the diagonal adjacency allows more closeness between nano-wires and gates, thus enhancing area utilization. This example highlights the importance of gate placement for efficient layout design.

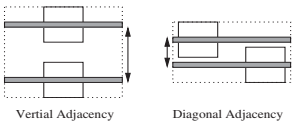

Figure 2: Effects of adjacency in gate design

Therefore, placement is a tight requirement for accomplishing closeness (diagonal adjacency) among gates. Figure 3 (a) shows a simple circuit made of three product terms, while Figure 3 (b) shows a possible modification to increase the closeness among nano-wires, thus effectively compressing the layout.

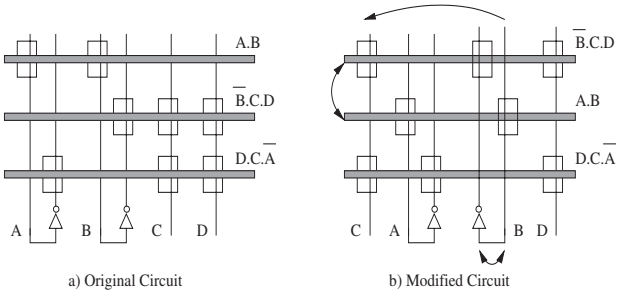

Figure 3: Increasing closeness among gates

3 Proposed Combinatorial Approach

As shown previously, modifications to the layout are required to overcome sizing differences; this process involves moving rows (product term nano-wires) and columns (gate lines). This can be solved using a graph approach in which each row/column is mapped to a graph node; an edge is placed between every pair of nodes (complete graph) with a weight given by the number of adjacent gates in the corresponding rows/columns. These graphs are referred to as adjacency graphs. Figure 4 shows the graph representations of the nano-circuit of Figure 3.

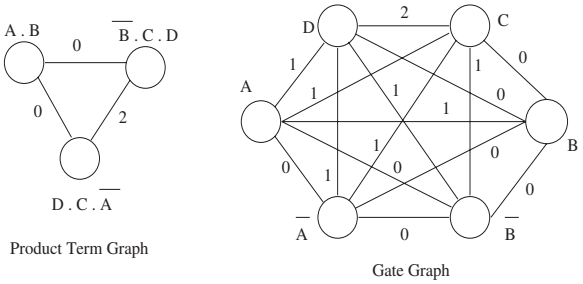

Figure 4: Adjacency graphs

The Minimum *Hamiltonian* cycle of these graphs corresponds to the optimal placement of the product terms (nano-wires or rows) and gates (columns). However, an optimum solution to this problem requires an exponential complexity (i.e. it is NP complete). The so-called Lin-Kernighan heuristic algorithm [11] is utilized in this paper; this algorithm has polynomial time with near optimal solution in most cases.

3.1 Example: the c17 benchmark

Consider a simple combinational circuit from the ISCAS85 benchmark set as shown in Figure 5. Each of the two outputs (g_{22} and g_{23}) can be expressed in SoP form of five inputs as,

$$g_{22} = g_1 \cdot g_3 + g_2 \cdot \overline{g_3} + g_2 \cdot \overline{g_6} \quad (1)$$

$$g_{23} = g_2 \cdot \overline{g_3} + g_2 \cdot \overline{g_6} + g_7 \cdot \overline{g_3} + g_7 \cdot \overline{g_6} \quad (2)$$

There are seven product terms, but two of them are redundant, i.e. they are used in both SoPs ($g_2 \cdot \overline{g_3}$ and $g_2 \cdot \overline{g_6}$). So, only five product terms must be implemented. In general, SoPs can be minimized using a 2-level logic optimization tool, such as Espresso [12]. The corresponding adjacency graphs can be constructed as in Figure 6. The arrow lines represent the solution to the combinatorial problems for an optimal gate placement. Figure 7 shows the original and the optimal implementations of the product terms for the c17 benchmark. The original circuit had 8 adjacencies, four of them are along the diagonals. The optimal circuit has only four adjacencies, all of them are in the diagonal directions.

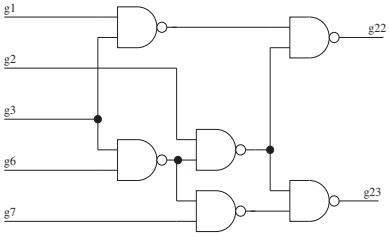

Figure 5: c17 benchmark netlist

4 Conclusion

This paper has presented an homogeneous (array-based) approach for designing and manufacturing digital circuits using nano-tubes/nano-wires. A methodology has been proposed for placement and reduced patterning effort for nano-wires to implement combinational circuits in Sum-of-Products (SoP) form. A combinatorial approach has been proposed for its solution; as an optimal technique has exponential complexity (due to NP completeness), an heuristic based technique with polynomial complexity has been presented for gate placement to reduce the area layout of the circuit.

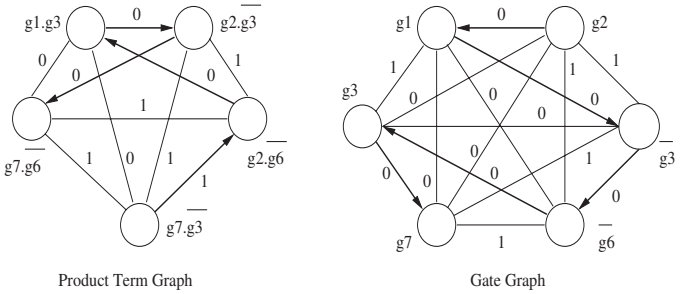

Figure 6: c17 benchmark adjacency graphs

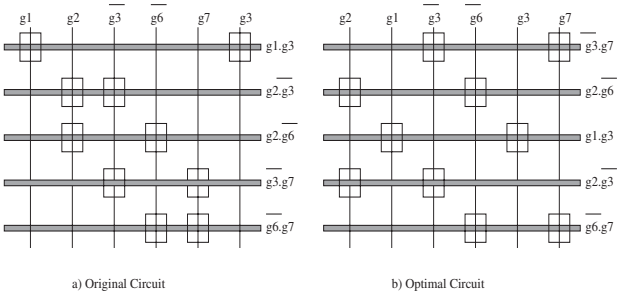

Figure 7: Optimal gate placement for c17

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