

RF Modeling for FDSOI MOSFET and Self Heating Effect on RF Parameter Extraction

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ABSTRACT

In this paper, a BSIMSOI RF gate resistance model for FDSOI MOSFET is introduced and verified. With the addition of the gate resistance model, the RF characteristic of FDSOI MOSFET could be modeled well. Self-heating effect (SHE) will affect RF data fitting significantly. A simple method to extract thermal resistance is proposed.

Keywords: SOI MOSFET, radio frequency, self-heating effect, compact model

1. INTRODUCTION

Silicon-on-insulator (SOI) technology is used for very large scale integration logic applications [1]. High performance microprocessors using SOI technology have been commercially available since 1998. SOI CMOS could offer a 20-35% performance gain over bulk CMOS [2]. In addition to the application in logic circuits, SOI technology is also attractive in low power microwave circuits because of its excellent performance in cutoff frequency [3]. Fully Depleted (FD) SOI MOSFET is promising for implementing radio frequency (RF) integrated circuits with low power consumption and low supply voltage [4]. However, one of the obstacles to fully exploiting the RF application of SOI technology is the lack of an accurate compact model capturing both the DC and high frequency characteristics of SOI MOSFETs. In this paper, we introduce BSIMSOI RF model for FDSOI device. The model is verified using devices fabricated at MIT Lincoln Lab. We also studied the self-heating effect on RF data fitting, and a

simple method to extract the thermal resistance is proposed.

2. BSIMSOI MODEL

In comparison with bulk MOSFET, SOI devices have some special characteristics such as the floating body effect (FBE) and the self-heating effect. To suppress the floating body effect, body contacts are used in some of the SOI devices. BSIMPD/BSIMSOI can model all the above phenomena [5], as well as other important physics, for example, gate to body tunneling current, impact ionization current. In addition, BSIMSOI dynamically captures the PD/FD transition [6], since SOI MOSFET can be either partially depleted or fully depleted depending on the bias voltages as well as doping concentration, thin silicon film thickness and size of the transistor.

To model the RF characteristics of FDSOI device, a BSIM4 compatible gate resistance model is implemented in BSIMSOI [5]. The gate resistance model includes two parts, one is the gate electrode and contact resistance; the other part is the intrinsic input resistance, in which both the drift and diffusion components of the channel conductance are included. The gate electrode and intrinsic input resistance are given by the following formula respectively:

$$R_{g\text{eltd}} = \frac{RSHG \cdot \left(XGW + \frac{W_{\text{eff}}}{3 \cdot NGCON} \right)}{NGCON \cdot (L_{\text{drawn}} - XGL)}$$

$$\frac{1}{R_{ii}} = XRCRG1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff} \mu_{eff} C_{oxeff} k_B T}{qL_{eff}} \right)$$

where *RSHG*, *XRCRG1*, *XRCRG2* are model parameters, and *NGCON* is the number of gate contact.

3. FDSOI MOSFET FABRICATION AND MEASUREMENT

To verify this RF model, we use it to model the FDSOI MOSFETs fabricated and characterized at MIT Lincoln Lab. The device we use has four fingers with width equal to 5um for each of the fingers. The channel length is 0.2um. The film thickness T_{si} is 40nm. The gate oxide thickness T_{ox} is 42 Å and the buried oxide thickness is 400nm. The DC measurement drain current and output conductance are shown in figures 1 and 2. The frequency range for S-parameter measurement we show here is from 45MHz to 20GHz, with gate biased at 0.8V and drain biased at 0.9V.

4. MODEL VERIFICATION

4.1 S22 Mismatch and Self-Heating

The DC drain current and DC output conductance fitting results are shown in figures 1 and 2 respectively. Initially, we found that S11 could be easily fit because of the gate resistance model, while S22 showed a large mismatch with the measured data even at low frequency (45MHz) as shown in figure 3. That means even though the DC output conductance is modeled well, the low frequency S22 parameter is still ill modeled. This is not the case in bulk MOSFET model, in which as long as the DC output conductance is correctly modeled, the low frequency S22 parameter will be match as well. In Fig. 3, S22 data shows higher conductance than the SOI model prediction.

In SOI device, the DC current and output conductance fitting is affected by self-heating effect impact ionization, channel length modulation. Impact ionization and channel length modulation increase the output conductance. Self-heating effect decreases the output conductance

because the mobility decreases with increasing drain bias as the temperature of the device increases. When the frequency approaches 1 MHz, the self-heating effect can not completely follow the high signal frequency and the conductance begins to increase as shown in figure 4. At 10's of MHz, the output conductance is totally free of the effect of self-heating and becomes frequency independent again. (The floating body effect can produce another step change in the frequency domain at a higher frequency but that may be insignificant in a FD device.). The amount of the conductance increase ΔG_{SHE} depends on the thermal resistance R_{th} . If the thermal resistance is underestimated in the DC case, the output conductance can still be fit well because other parameters such as channel length modulation parameters can make up for the error of in R_{th} . However when it comes to RF data fitting, the lower R_{th} would cause under prediction of the rise in conductance at MHz. That is the case of S22 misfitting in Fig. 3.

So the accurate extraction of thermal resistance for self-heating is essential for RF modeling. An inaccurate thermal resistance may be unobvious in DC fitting but hurt RF significantly.

4.2 Thermal Resistance Extraction

To extract the thermal resistance, an AC method has been proposed before [7]. From the analysis above, to fit S22 parameter, we care mostly about the thermal resistance rather than the thermal capacitance, therefore, here we propose a simple method to extract R_{th} . The junction diode current is used as a thermometer to set a relationship between the temperature and the power consumption. The measurement setup for diode~temperature and diode~power consumption are shown as Fig. 5. The junction diode current increase with the temperature is shown in Fig 6(a). The diode current will also change with power consumption of the device as shown in Fig 6(b). R_{th} is therefore derived from

$$R_{th} = \frac{d \log(I_{BS}) / dP}{d \log(I_{BS}) / dT}$$

To find the thermal resistance parameter R_{th0} used in BSIMSOI model, R_{th} is multiplied by the width of the transistor, since

$R_{th} = R_{th0} / W_{eff}$ [5]. After a correct extraction of R_{th} , all S parameters could be fit very well as shown in Fig. 7.

5. CONCLUSION

Without using the body resistance network, RF characteristic of FDSOI MOSFET is well captured by BSIMSOI gate resistance model. Self-heating effect plays an important role in RF parameter extraction therefore the thermal resistance needs to be accurately extracted. A simple method for thermal resistance extraction has been proposed. It is worth noting that while self-heating must be carefully corrected during parameter extraction, self-heating effect does not have to be invoked during high clock rate digital circuit simulation because of the tiny average power dissipated in each digital transistor. One can take advantage of this realization to speed up digital circuit simulation. However, in RF/Analog circuits, high and low frequency may coexist, therefore, self-heating effect cannot be ignored.

REFERENCE

- [1] C.T. Chuang, P.F. Lu, C.J. Anderson, "SOI for Digital CMOS VLSI: Design Considerations and Advances", Proc. IEEE, Vol.86, No.4, pp689-720, 1998
- [2] G.G. Shahidi, "SOI Technology for the GHz era", IBM J. Res. & Dev. Vol. 46, No. 2/3, pp. 121-131, 2002
- [3] D. Flandre, J.P. Raskin, D. Vanhoenacker-Janvier, "SOI CMOS Transistors for RF and Microwave Applications", Int. J. High Speed Electronics and Systems, Vol. 11, No.4, 2001
- [4] Y. Taur, "CMOS Scaling into the Nanometer Regime", Proc. IEEE, Vol. 85, pp. 486-504, Apr. 1997.
- [5] BSIMPD/BSIMSOI User's Manual and website <http://www-device.eecs.berkeley.edu/~bsim3soi>

[6] P. Su, S. Fung, P. Wyatt, H. Wan, M. Chan, A. Niknejad and C. Hu, "A Unified Model for PD and FD SOI Circuit Designs: Using BSIMPD as a Foundation" Proc. IEEE CICC, 2003, pp. 241-244.

[7] W. Jin, W. Liu, S.K.H. Fung, P.C.H. Chan, C. Hu, "SOI Thermal Impedance Extraction Methodology and Its Significance for Circuit Simulation", IEEE TED, vol.48, No.4, pp.730-736, 2001

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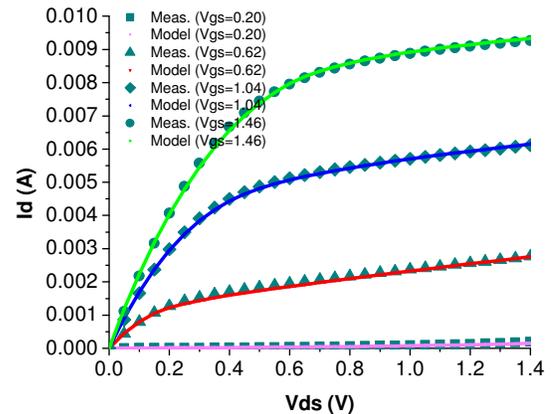


Figure 1: DC fitting of drain current
($W/L = 4 \times 5 \mu\text{m}/0.2$)

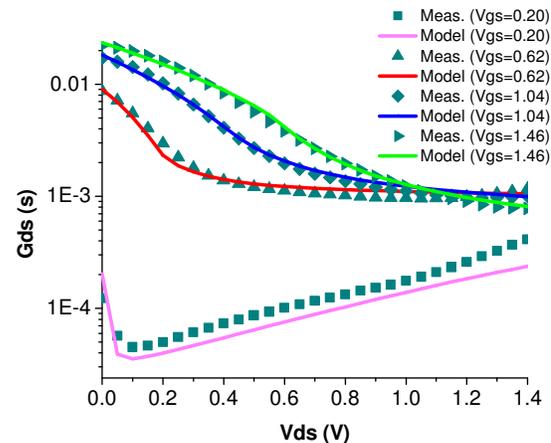


Figure 2: DC fitting of output conductance
($W/L = 4 \times 5 \mu\text{m}/0.2$)

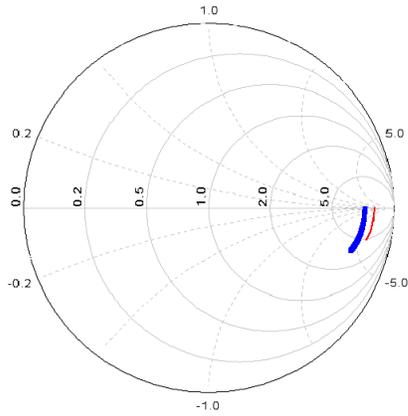


Figure 3 Poor S22 fitting. The blue symbol (thick stars) is data, the red symbol is model prediction. Even though dc output conductance is well fit, S22 is underestimated.

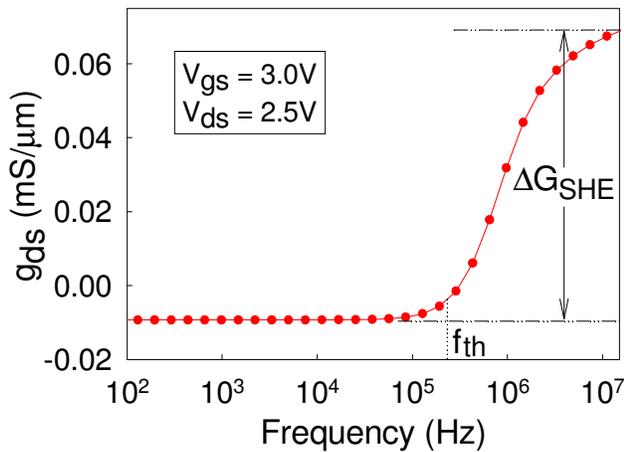


Figure 4 Self-heating effect on g_{ds} , between about 0.2 and 20 MHz or even larger, the AC self-heating effect gradually disappears because it cannot follow the rapid signal change and the G_{ds} increase to the AC-heating free value.

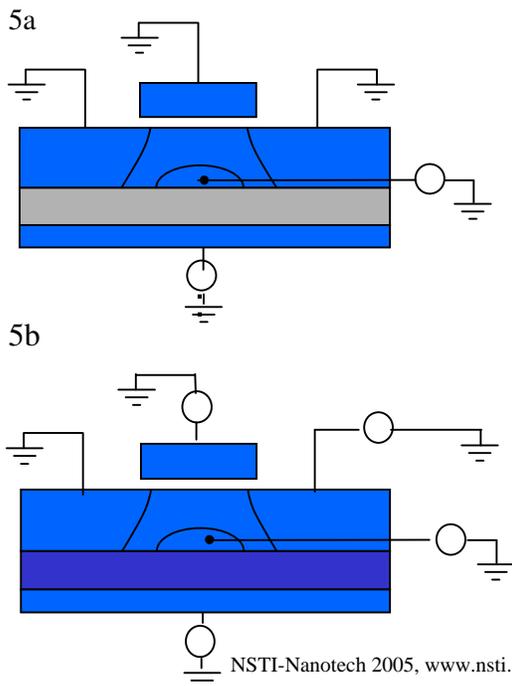
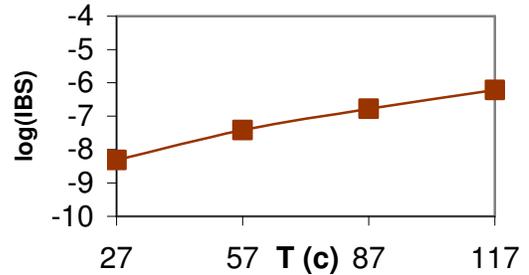
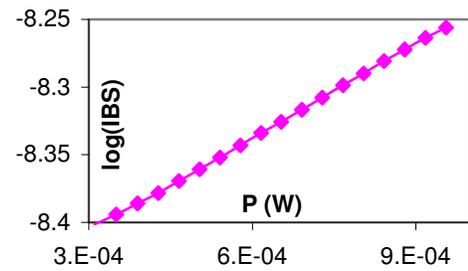


Figure 5 R_{th} extraction setup
 (5a) biasing condition to measure $d\text{Log}(I_{bs})/dT$, $V_{sub}=-10V$, $V_{bs}=0\sim 1V$, device is off;
 (5b) biasing condition to measure $d\text{Log}(I_{bs})/dP$, $V_{sub}=-10V$, $V_{bs}=0.6\sim 0.9V$, device is on;



6a



6b

Figure (6a) Measurement result of figure 5a $\log(I_{bs})$ vs. T;
 (6b) Measurement result of figure 5b $\log(I_{bs})$ vs. power

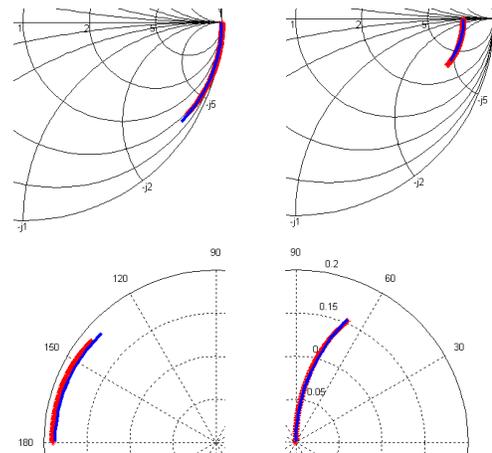


Figure 7 S parameter fitting after correctly extracting the thermal resistance. (Left top: S11; Right top: S22; Left bottom: S21; Right bottom: S12)