Device Parameter Extraction from fabricated Double-Gate MOSFETs

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ABSTRACT

We have successfully conducted the device simulation of Double-Gate MOSFET (DG-MOSFET) in good agreement with electrical characteristics of the fabricated 105-nm DG-MOSFET, by fitting only a shape parameter of Gaussian doping profile using a conventional device simulation model, for the first time. The agreement can be considered to be due to the good characteristics of the fabricated DG-MOSFET with ideal rectangular fin cross section. The simplification of the device simulation model is also possible due to the immunity of SCE of the fabricated DG-MOSFET. The device parameters have been extracted from the fabricated DG-MOSFET by the simplification of the conventional device simulation model, such as source-drain resistance evaluation and step doping profile approximation. The device parameter fitting and the device model simplification of the good performance DG-MOSFET are promising for realizing physical-based spice simulation of DG-MOSFETs.

Keywords: device parameter extraction, Double-Gate MOSFFETs, device simulation, device modeling

1 INTRODUCTION

With advancement of the scale down Silicon (Si) technology, DG-MOSFETs have been received much attention to open a new Silicon device stream. Because DG-MOSFETs have the excellent structures which can suppress short channel effect (SCE), even less 20-nm MOSFETs. Therefore, DG-MOSFETs are the most promising devices in region of future extreme miniature-size. That's why the fabrication technology, device simulation, and device modeling of the DG-MOSFETs are in the hot research stage. Although many research results have been reported ([1], [2]), spice simulation of DG-MOSFET's device model has been not realized in good agreement with characteristics of the real devices. Such accurate spice simulation needs parameter extraction from the fabricated DG-MOSFETs with good electrical characteristics, and development of physical-based spice simulation model. It is very difficult to fabricate such good DG-MOSFETs, so that device parameter extraction from fabricated DG-MOSFETs has been not reported yet.

A silicon nanoscale devices group of AIST (Advanced Institute of Advanced Industrial Science and Technology) successfully already fabricated ideal fin-type DG-MOSFETs enough to extract device parameters ([3]). The fabricated DG-MOSFETs have high performance (immunity of SCE, S ≅ 60mV/dev, high drivability) and ideal flat channel surfaces (like bulk surface).

We have tried to extract prime device parameters from electrical characteristics of the fabricated DG-MOSFET. The simplification of device simulation model of the fabricated DG-MOSFET has been considered for development of spice simulation model.

2 FABRICATED DG-MOSFET

Some of authors successfully fabricated n-DG-MOSFET as shown in Fig. 1. The fabricated DG-MOSFET has a gate length of 105 nm, a Si thickness of 13 nm, and two oxide thickness of 2.2 nm. The Si-Fin height of 82 nm denotes the Si channel width. The ideal rectangular cross-section Si-Fin channel was formed using excellent technology of electron beam (EB) lithography and isotropic wet etching process. The fabricated real device has ideal

flat channel surfaces, and shows excellent characteristics shown in Fig. 2(b)-5(b). A short channel effect is well suppressed in the fabricated DG-MOSFET. It is noted that the drain currents of the Id-Vd characteristics are values when the channel width is 1 μm.

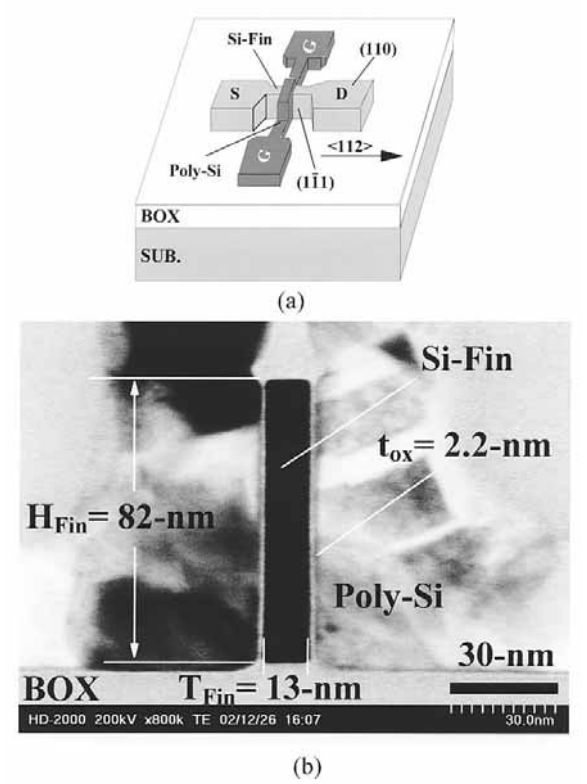


Fig.1 (a) Three-dimensional schematic diagram of the fabricated DG-MOSFET, and (b) cross-sectional TEM image of the measured DG-MOSFET ([2]).

3 DEVICE PARAMETER EXTRACTION

3.1 Conventional Device Simulation Model

We have optimized device parameters of two-dimensional Atlas device simulation of SILVACO International, Inc ([4]), so that the simulation data was corresponding to the measurement data of the fabricated DG-MOSFET. For optimizing the device parameters, SILVACO's automatic device parameter fitting tool, Optimizer was employed ([5]). The Optimizer executes Atlas device simulation repeatedly changing the device parameter values little by little, until the simulation data give close agreement with measurement data of the fabricated device.

First, we have assumed a device simulation model with Gaussian doping profile and source/drain wires that is faithfully close to the fabricated device as shown in Fig. 2(a). We refer to this model as device simulation model A. Drift diffusion model and field dependent (CVT) model were used as transport model and mobility model, respectively. The contact resistances can be ignored, because the contact size of the fabricated device is very large.

As the surface doping concentration of the fabricated device was 10^{20} cm^{-3}, the shape of Gaussian doping profile was the only fitting parameter. The other device parameter was default of Atlas device simulator. As shown in Fig.2(b), we have succeed in matching curves of the simulation characteristics to those of the measured characteristics, by optimizing only a Gaussian shape parameter, for the first time. The shape parameter is specified by the characteristic length of Gaussian doping profile in the Atlas simulator. The optimized characteristic length is 3.61 nm.

We have found that device parameter fitting is possible even in the 105-nm DG-MOSFET using conventional device simulation model. It can be considered that the agreement between simulation data and measurement data shows the good performance of the fabricated DG-MOSFET.

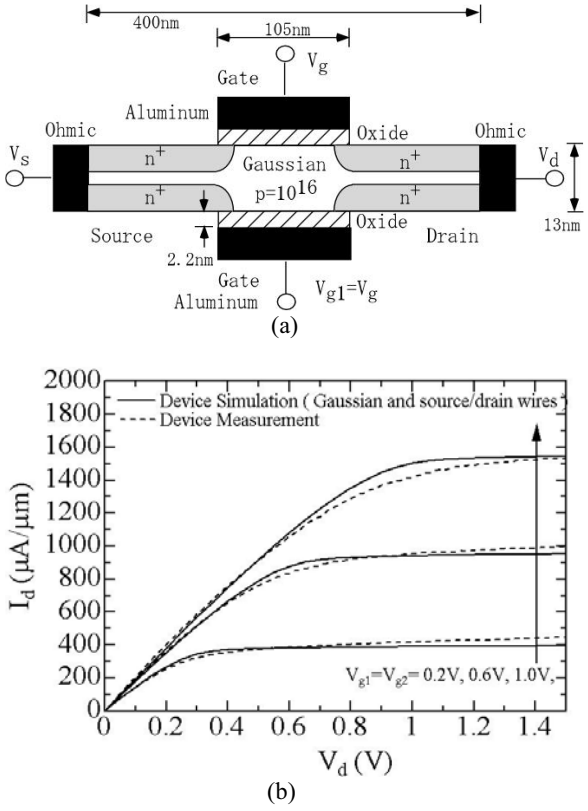
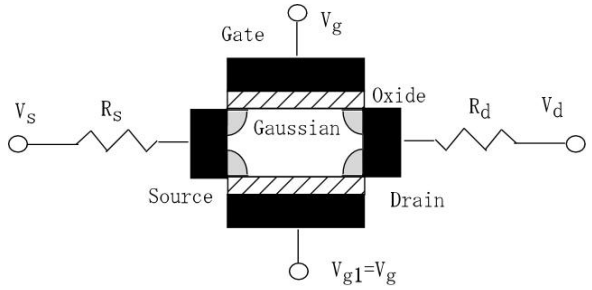


Fig.2 (a) device simulation model A with Gaussian doping profile and source/drain wires, and (b) Comparison of Id-Vd characteristics between real device measurement and device simulation with the model A.

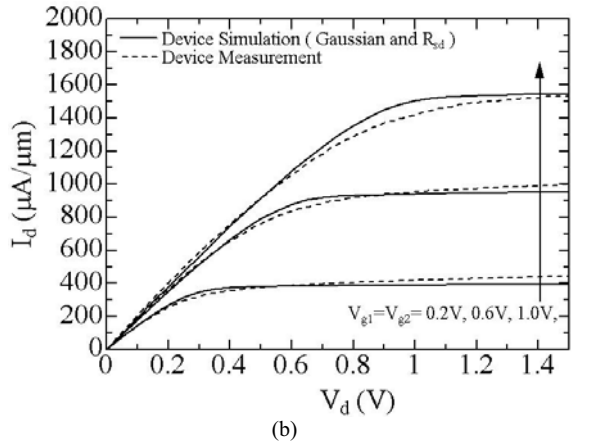
3.2 Source-drain Resistance Evaluation

Next, in order to extract source-drain resistance parameter, we have introduced the device simulation model B with source and drain resisters instead of source and drain wires of the above-mentioned device simulation model A. (Fig. 3(a))

As shown in Fig. 3(b), we have successfully optimized source and drain resisters in good agreement with the measured data without changing the other optimized device parameters of the device simulation model A. The optimized source and drain resistances were optimized to 212 Ω μm, respectively.



(a)



(b)

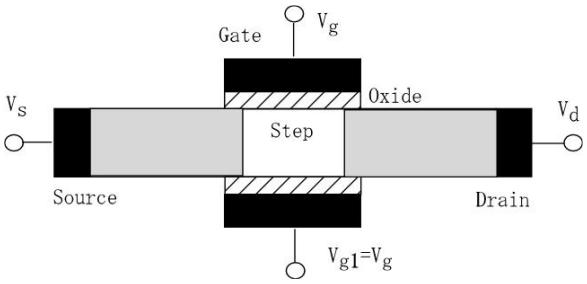
Fig.3 (a) device simulation model B with Gaussian doping profile and source/drain resistances, and (b) Comparison of Id-Vd characteristics between real device measurement and device simulation with the model B.

3.3 Step Doping Profile Approximation

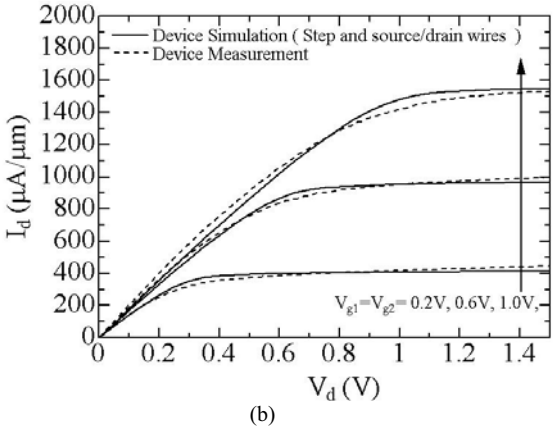
Then, in order to investigate whether effective channel length parameter can be extracted, we have introduced the device simulation model C with step profile instead of Gaussian profile of the above-mentioned device simulation model A. (Fig. 4(a))

As shown in Fig. 4(b), we have successfully optimized the concentration and distance the source and drain step doping profile so as to agree with the measured data without changing the other optimized device parameters of the device simulation model A. The optimized concentration and distance are 4.23 x 10^{19} cm^{-3} and 77.1 nm, respectively.

It was found that Gaussian doping profile is fairly well approximated by step doping profile, although the rising slope in the linear region is a little different. This experimental result indicates that the barrier height near source edge is not affected so much by drain potential, because source electric field is fairly shielded from drain electric field by double gate bias in the fabricated device.



(a)



(b)

Fig.4 (a) device simulation model C with step doping profile and source/drain wires, and (b) Comparison of Id-Vd characteristics between real device measurement and device simulation with the model C.

3.4 Simple Device Simulation Model

Finally, in order to simplify device simulation model, we have developed the device simulation model D with step doping profile and source/drain resistances, with which the device simulation model B and C were combined. (Fig. 5(a)) The all device parameters are same as the optimized values of the device simulation model B and C.

Figure 5(b) shows device simulation result using the simple device simulation model D. The simulation data agree with the measure data permissibly. This result accords with results using device simulation model B and C. A little difference between two data sets dues to non-linear

source and drain resistances. The non-linear effect of source and drain resistances should be considered in spice device simulation.

Because DG-MOSFETs are suitable for simplification of the device simulation model for the immunity of SCE, the device simulation model A for device simulation can be simplified to the model simulation model D for spice simulation, when nonlinearity of source and drain resistances is considered. The simplification of device simulation model is effective for the development of spice simulation model. This result contributes to the realization of spice simulation of DG-MOSFETs that gives close agreement with behavior of real DG-MOSFETs.

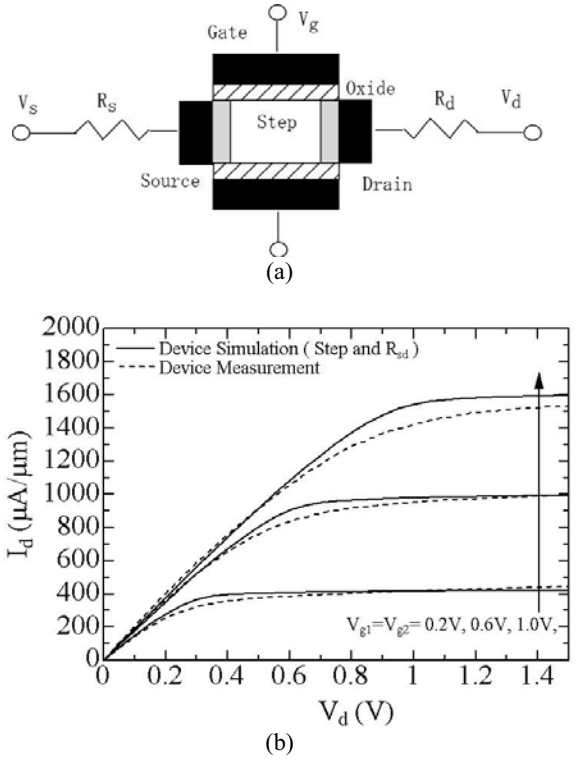


Fig.5 (a) device simulation model D with step doping profile and source/drain resistances, and (b) Comparison of Id-Vd characteristics between real device measurement and device simulation with the model D.

4 CONCLUSION

The device simulation of the DG-MOSFET has successfully been conducted in good agreement with characteristics of the fabricated 105-nm DG-MOSFET, by fitting only a shape parameter of Gaussian doping profile of the conventional device simulation model, for the first time. The agreement shows excellence of the fabrication technology and the device performance.

It has been confirmed experimentally that source/drain wires and Gaussian doping profile can be approximated to source/drain resistances and step doping profile in the fabricated 105-nm DG-MOSFET, respectively. The DG-MOSFETs are suitable for simplification of the device simulation model for the immunity of SCE. The device prime parameters have been successfully extracted using simplification of the conventional device simulation model.

The device parameter fitting and the device model simplification of the fabricated DG-MOSFETs are attractive for realization of spice simulation of DG-MOSFETs. Three-dimensional device simulation and advanced device simulation model are needed for matching simulation characteristics to measured characteristics with more accuracy.

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