Airgap and Line Slope Modeling for Interconnect

F. Badrieh and H. Puchner

Cypress Semiconductor, 3901 N. First Street, San Jose, CA 95134, fib@cypress.com

ABSTRACT

Interconnect is becoming more critical for integrated circuit performance for both memory and logic devices. Backend delay is a significant portion of both routing delay and cell delay. With shrinking dimensions, interconnect lines get closer, resulting in larger coupling and fringing capacitance. For example, line-to-line space for a 65 nm node technology can be as small as 0.11 μm. At these small dimensions, every facet of the manufacturing process matters in modeling interconnect capacitance. Of particular importance are airgaps forming between lines and line slopes – both of which are space dependent. In this work we have developed and applied a generic methodology for capturing void and slope features, based on silicon data, modeled them using a field solver, and utilized their simulation output for potential use in circuit design.

Keywords: Interconnect, voids, airgaps, capacitance

1 INTRODUCTION

Aluminum-TEOS process has the following two known features: (1) Airgaps (voids) form between metal lines during PECVD (plasma-enhanced chemical-vapor deposition), and (2) metal lines tend to have a defined slope as a function of space. Copper/low-k process, on the other hand, while it has space-dependent line slope, it requires additional steps to intentionally add voids between metal lines. The impact of voids in both cases is huge, especially at small space. Since voids are formed from air, and air has a low-k dielectric constant (k=1), voids result in significantly lower capacitance, sometimes up to 30% smaller than the no-void case. Consequently, modeling voids is of great importance. The difficulty in modeling voids stems from the fact that their shape, volume and altitude varies as a function of space. At large space they eventually vanish.

Line slope on the other hand becomes important at moderate-to-large space. It is at this space the bottom CD of an Aluminum/TEOS process could become significantly larger than top CD. (Copper/low-k, on the other hand, exhibits slopes in the other direction – e.g., top CD is larger than bottom CD.) For example, an Aluminum/TEOS 0.14 μm line may have bottom CD twice as wide as top CD. If such a line routes right above a plate, an effectively wider line would couple stronger to the bottom plate. Therefore, it is important to model line slope as a function of space.

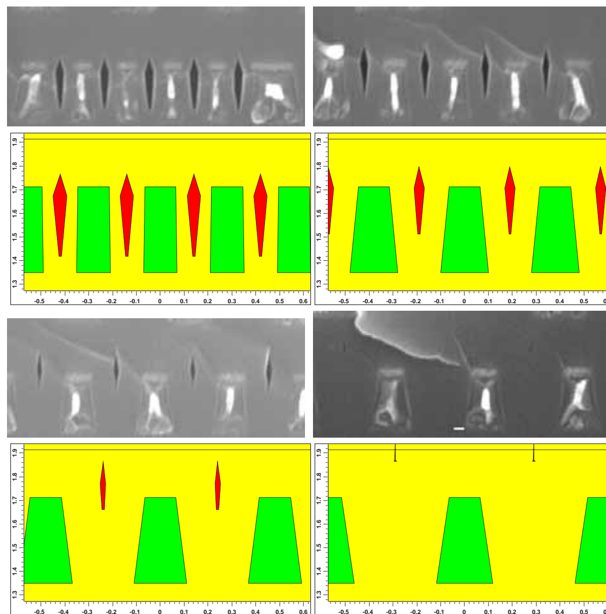

Figure 1: SEM and corresponding simulation images of 3.5K Aluminum lines at small space (0.14 and 0.24 μm) and at larger space (0.34 and 0.44 μm).

2 SILICON BASED VOID MODELS

The methodology introduced is based on having a void-characterization test structure, measuring void dimensions as a function of space by cross-sectioning the test structure, fitting into a model and feeding the model into the field solver engine. We illustrate the method with three examples.

The first example shows a 3500 $\AA$-thick aluminum line. The SEM images in Figure 1 show metal lines at different spaces, starting from 0.14 μm with increments of 0.10 μm. The images show metal and ILD profile as a function of space. The voids (airgaps) are clearly visible in such a process architecture. The void position and shape varies versus space – the void maximizes at

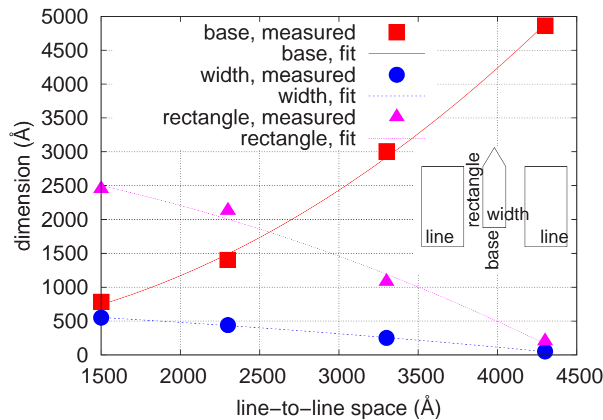

Figure 2: 3.5K Aluminum line void measured dimensions and corresponding fit functions versus space.

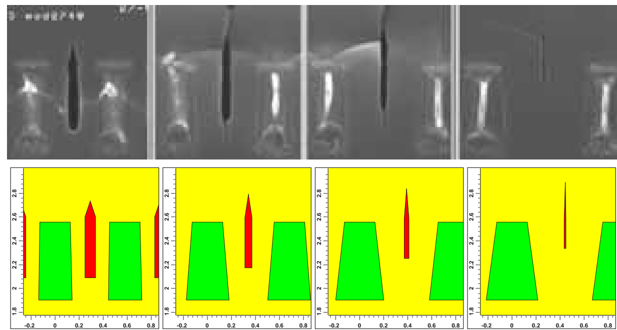

Figure 3: SEM and corresponding simulation images of 6.5K Aluminum lines as a function of space (0.30, 0.40, 0.50 and 0.60 μm).

minimum space and vanishes at large space.

At each space void width, height and altitude (base) are measured. The measured data is subsequently fitted to a function in the form $a+bx+cx^2$, where x is the line-to-line space and a, b and c are fitting constants (which will be different for each of width, base and height). The measured data for this particular thickness as well as the fitting functions are shown in Figure 2. Notice how the base of the void rises versus space, and both void width and thickness decrease versus space.

The fitting functions may then be embedded in a field solver accounting for metal thickness, profile, conformal dielectrics, and airgaps for typical backend stacks as well as fast and slow corners. Sample simulation outputs are also shown in Figure 1. Since metal and void profile match silicon pretty well, one is assured that the corresponding capacitance simulation results fit silicon extracted data within high accuracy ($\sim \pm 5\%$).

The second example is a 6500 $\AA$ aluminum line. Top of Figure 3 shows SEM images at different spaces. Bottom of same figure shows corresponding simulations structures. Since the metal is thicker, the void is larger.

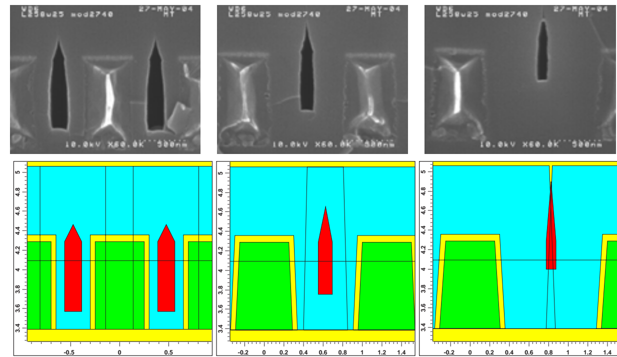

Figure 4: SEM and corresponding simulation images of 8.5K Aluminum lines as a function of space (0.45, 0.75 and 1.15 μm).

The last example is an 8500 $\AA$ Aluminum line. This kind of thick metal is generally used as top metal for power routing. This case differs from the above two cases in that top metal has a subsequent passivation step. Passivation maybe a thin layer of oxide followed by a thick layer of nitride. Figure 4 (top) shows SEM images at different spaces and (bottom) corresponding simulations structures.

2.1 Void Sensitivity Analysis

Void sensitivity depends on the following: (1) dielectric constant – A void in nitride (k=7.5) has a larger impact on capacitance than a void in oxide (k=3.9). The reason is that in the former case capacitance reduction follows a factor of 7.5/1.0 (where the 1.0 is the k-value of air), while in the latter case it follows a factor of 3.9/1.0. (2) Space range – a void between two lines at minimum space has a much larger impact on capacitance than the same void between two lines at larger space. Take for example a 500 $\AA$ void between two lines at 1000 $\AA$ separation. Compare this to the same void at 2000 $\AA$ separation. In the former case, air is 50% of ILD, while in the latter case it is only 25%. The implication of this is that voids become very important for current- and next-generation backends. (3) Void volume and altitude – as shown above void width decreases at large space and void altitude increases. A narrower void will have less of an impact and so does a higher altitude void.

2.2 Impact of Void on Capacitance

It is known that airgaps decrease capacitance. The reason is that voids contain air, which has the low-k value of 1.0. Physically what happens is that the introduction of voids increases the electric field inside the void, and reduces it at the surface of the metal. Since capacitance is the ratio of charge to voltage, and since charge is the surface integral of electric field around the

NSTI-Nanotech 2005, www.nsti.org, ISBN 0-9767985-3-0 WCM, 2005

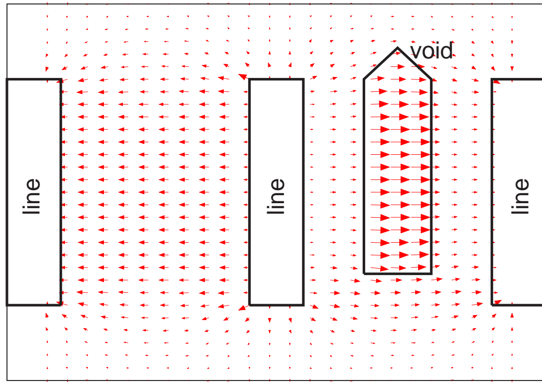

Figure 5: Electric field between lines without (left) and with (right) airgaps.

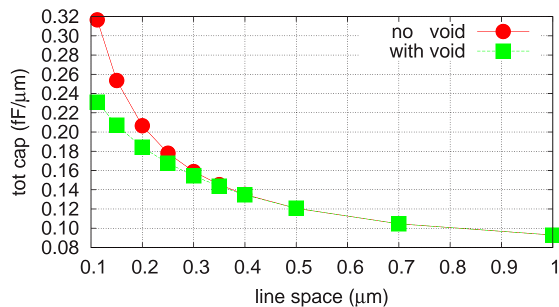

Figure 6: 3.5K metal capacitance, without and with voids (simulations).

metal, capacitance decreases. Figure 5 shows electric field without (left) and with (right) the airgap.

Figure 6 shows metal/field capacitance as a function of space, both with and without voids. We notice that at a minimum space of 0.11 μm the presence of voids dramatically decreased capacitance by 30%. This may have a huge impact on timing delays. On the other hand, at large space the void vanishes and both curves merge. For the particular metal sample at hand, the void is completely vanished at 0.4 μm. For thicker metals (e.g., Figure 4) voids may persist up to spaces even beyond 1 μm.

3 SILICON BASED LINE SLOPE MODEL

The second part of this work relates to metal slope. Since previous sample images were decorated it is relatively hard to see line slope. A clearer TEM image (for the 3.5K case) is shown in Figure 7. One can see that at a top space of 245 nm the line is almost vertical; at a top space of 478 nm there is a more defined slope; and at 927 nm space there is a very clear slope. The difference between top CD and bottom CD, as a function of space (divided by two) is shown in Figure 8. The data maybe fitted into an equation of the form $a - be^{-cx}$, where again x is line space and a, b and c are fitting constants.

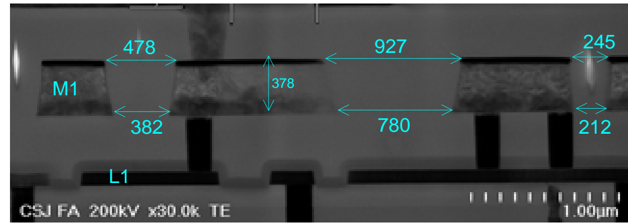

Figure 7: Sample TEM image showing metal slope as a function of space.

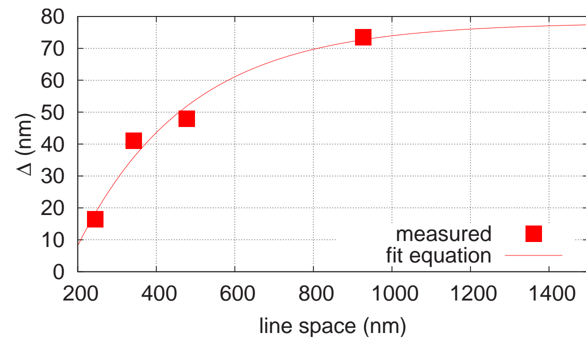

Figure 8: Bottom CD in Figure 7 is larger than top CD by twice Δ.

3.1 Line Slope Sensitivity Analysis

Line slope sensitivity depends on the following factors: First line width – the narrower the line the larger the impact of line slope. For example, it was observed that bottom CD of an isolated 3.5K line is wider by 0.07 μm on each side. A narrow line of target CD of 0.14 μm would therefore have a bottom CD of 0.28 μm, which is 100% larger than top CD. On the other hand a line with target CD of 1.00 μm would have a bottom CD which is only 14% larger than top CD. The second factor is line space – generally line slope becomes important at large space. As was noted and shown above lines at small space do not suffer from line slope, whereas isolated lines have significant slopes. The last factor is ILD thickness beneath the metal – as will be shown in the following subsection the thinner the ILD the larger the impact of line slope.

3.2 Impact of Line Slope on Capacitance

Figure 9 shows metal/over plate capacitance as a function of space, both including and excluding line slope information. The ILD underneath the metal is 2650 $\AA$ thick. We can see that at small space there is

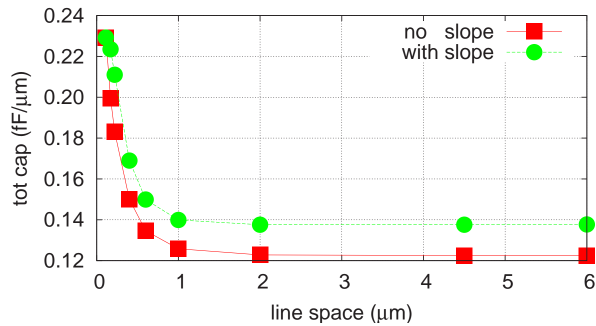

Figure 9: 3.5K line capacitance with and without line slope as a function of space (simulations).

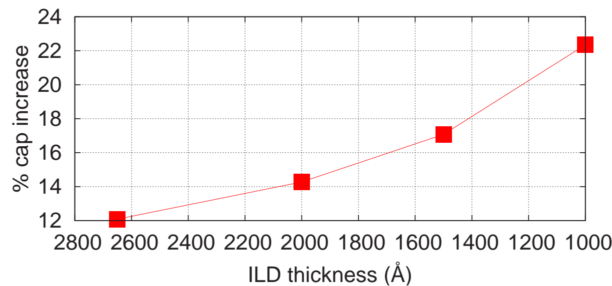

Figure 10: 3.5K line capacitance % increase (as a result of line slope) as a function of ILD thickness (simulations).

no difference between the curves. There, the line is almost vertical. At larger space we notice that the sloped case results in larger capacitance, sometimes by up to 12%. It is worth noting that the increase in bottom CD also has an impact on coupling capacitance, since it translates to a decrease in space.

Figure 10 shows percentage increase in capacitance (with-slope case versus no-slope case, and at large space) as a function of ILD thickness. It is very clear that line slope plays a larger role for thinner ILDs.

4 COMPARISON to OTHER METHODS

Since we are using analytical fitting functions for both void and line slope models then by definition this is an empirical method. In other words, no process/analytic simulations are employed. This is in contrast to earlier work we presented in [1] and [2] where we used a process simulator to predict void shape. The empirical method has proven to be very useful for different applications. It enables the modeling engineer to fully characterize voids and line slope. There are many kinds of fit functions which can be used and which can be inserted as-is in the field solver software. It is also possible to capture some process variations effects on capacitance. (For example, a worst case scenario line-space where lines print closer on silicon is automatically included in the void model, since the model allows one to interpolate versus space. The effect on capacitance of such a variation is therefore taken into account.) However, the empirical method comes with some drawbacks. It is assumed that (1) silicon process is stable and calibration images are representable; (2) multiple test structures (simple lines at various spaces) have to be defined and characterized; (3) availability of SEM images and (4) corner models are independent of line thickness. Items (1) through (3) would also be needed if one does process-simulations of void/line slope, because even then one needs SEM images to calibrate the simulator first. As for line thickness variation, one would have to either optimize the void model or conduct a DOE versus line thickness to add this parameter to the empirical model.

Complicated 3-dimensional structures such as dense SRAM memory cells are very difficult to simulate employing an empirical void/line model. Process simulators are the only reasonable method to be used in this case. However, process simulation can only automate the geometry impact and still has to be calibrated to silicon experiments in order to predict the exact void shape and position.

5 CONCLUSION

We have devised a generic methodology for characterizing airgaps and line slope and including those features in interconnect modeling. The method is silicon-based and can be used to accurately model the impact on capacitance. Our main conclusion is that airgaps result in a significant reduction in capacitance at smaller space. Metal slope on the other hand kicks in at moderate-to-large space and results in an increase in capacitance.

REFERENCES

[1] C. Heitzinger et al., IEEE Transactions on Electron Devices, Vol. 51, No. 7, pp. 1129-1134, 2004.
[2] F. Badrieh et al., ESSDERC 2003, pp. 441-444.