The Surface-Potential-Based model HiSIM-SOI and its Application to 1/*f* Noise in Fully-Depleted SOI-MOSFETs

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Abstract

The fully-depleted SOI-MOSFET model HiSIM-SOI for circuit simulation is the first model for circuit simulation based on a complete surface-potential description. HiSIM-SOI solves the surface potentials at all three SOI-surfaces perpendicular to the channel surface self-consistently. Besides verification against measured *I-V* characteristics, HiSIM-SOI is also verified with a 1/*f* noise analysis, sensitive to the carrier concentration and distribution along the channel. During the noise analysis, it was found that the carrier concentration increase in SOI-MOSFET leads to an enhanced 1/*f* noise in comparison with the bulk-MOSFET. Therefore, HiSIM-SOI predicts that further reduction of the silicon-layer thickness necessary for achieving higher driving capability will cause unavoidable noise enhancement.

Keywords: SOI-MOSFET, HiSIM-SOI, surface-potentail-based model

1 Introduction

MOSFET is the most widely applied device, and possible future variations such as double-gate MOSFET as well as

FinFET have been intensively investigated [1,2]. Our objective is to develop a circuit simulation model for the fully-depleted SOI-MOSFET as the first step for describing phenomena caused by the channel confinement between two oxide layers, which will be the case for most of these future devices.

Existing SOI-MOSFET models are suffering convergence problems in circuit simulation. The main reason is a violation of the charge conservation. The SOI-MOSFET has three Si-SiO_2 surfaces as can be seen in Fig. 1, and thus charges are induced at all surfaces. To include all these charges in the model the surface-potential-based modeling is the only solution to secure the charge conservation in a consistent way [3]. Here a question arises whether computational efficiency can be achieved, which is important for real applications. Additionally, it is known that also numerical simulators suffer from the convergence problem even on the device-simulation level.

To realize suppressed simulation time as well as stable convergence for circuit simulation, we have solved precisely only for bias conditions influencing circuit performances and have applied further simplifications for trivial conditions [3]. The model was named HiSIM-SOI and is based on the charge conservation guideline. Obtained good agreement of calculated *I-V* characteristics with measurements proved the reliability of the method.

It is know that the carrier distribution along the channel plays an important role for second-order phenomena such as the noise as well as the non-quasi-static effect. To investigate carrier density modification in the SOI channel in comparison to the bulk-MOSFET, we thus focus on the investigation of the 1/*f* noise characteristics, of which the carrier concentration as well as its density distribution in the channel are requested in the modeling [4].

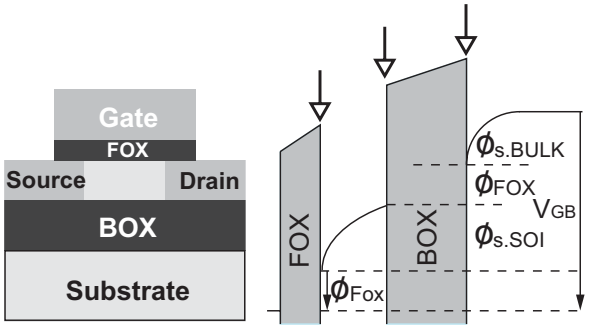


Fig. 1. Schematics of the fully-depleted SOI-MOSFET;(a) a structure, and (b) cross-sectional band diagram. The three involved surface potentials are solved iteratively with the Poisson equation.

2 Framework of HiSIM-SOI

In the surface-potential-based modeling, all device characteristics are described as functions of the surface potential. To include all device features of the

SOI-MOSFET consistently, HiSIM-SOI considers not only the surface potential at the channel surface, but also at the back side, as well as at the bulk back-gate. All 3 surface potentials are solved simultaneously with the Poisson equation as schematically depicted in Fig. 1. The simultaneous potential calculation for these three surfaces requires only about twice as much calculation time as for the bulk-MOSFET case, solving just at the channel-surface. Fig. 2 demonstrates the accuracy of the three calculated surface potentials in comparison to the results with the 2D numerical device simulation. Fig. 3a compares HiSIM-SOI simulation results of the channel-inversion charge with a 2D numerical simulation result for the silicon-layer thicknesses T_{SOI} of 50nm [6]. The bulk-MOSFET result is also depicted for comparison in Fig. 3a. Enhancement of the carrier concentration in the SOI case is obvious. Reliability of HiSIM-SOI has been proved down to a silicon-layer thickness of T_{SOI} of 25nm with a 2D-numerical simulator as depicted in Fig. 3b.

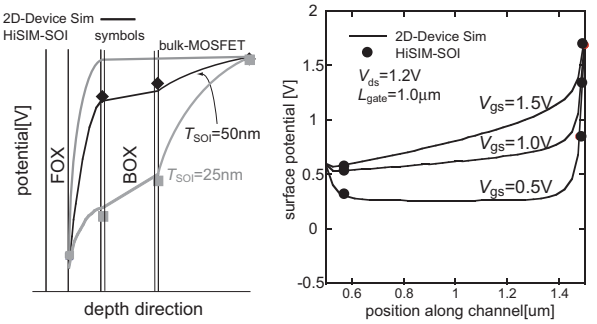
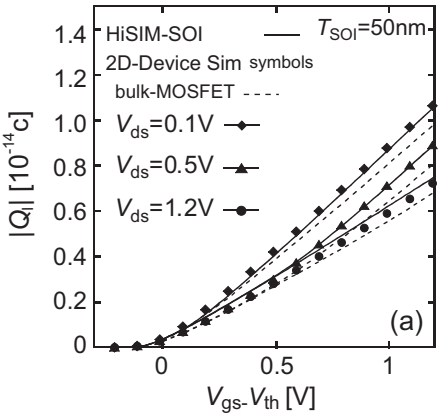


Fig. 2. Comparison of HiSIM-SOI calculated surface potentials with the results of a 2D-device simulator.



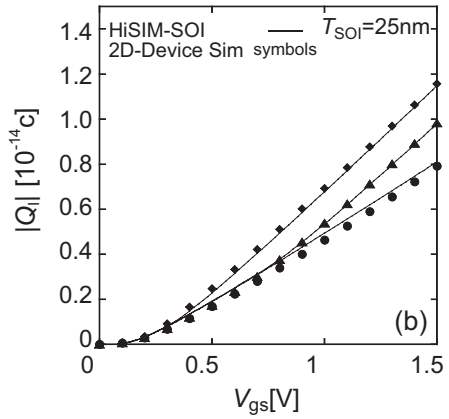


Fig. 3(a). Comparison of calculated inversion charge Q_I with 2D-device simulation results, for a silicon-layer thickness of 50nm. The bulk-MOSFET result is also plotted. (b). Comparison of calculated inversion charge Q_I with 2D-device simulator results, for a silicon-layer thickness of 25nm.

We have done parameter extraction for HiSIM-SOI from measured *I-V* characteristics of SOI transistors with T_{SOI}=50nm oxide-layer thickness. As shown in Fig. 4, good agreement has been obtained even with the bulk mobility model. Stable convergence in circuit simulation has also been proved. Fig. 5 demonstrates a simulation result of a ring oscillator.

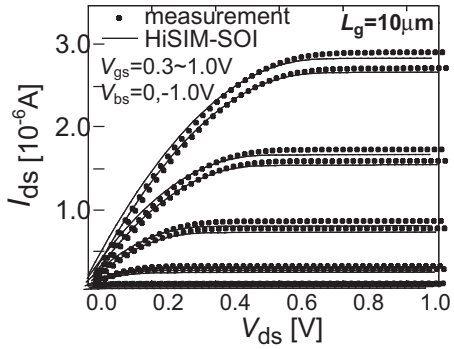


Fig. 4. Comparison of measured *I-V* characteristics(dots) with HiSIM-SOI(lines) results.

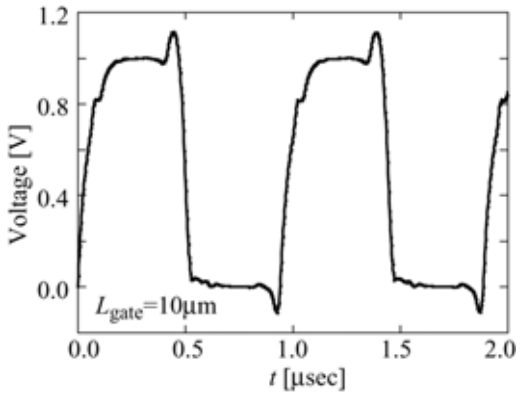


Fig. 5. Simulation result of a 5-stage ring oscillator using SOI MOSFET with HiSIM-SOI.

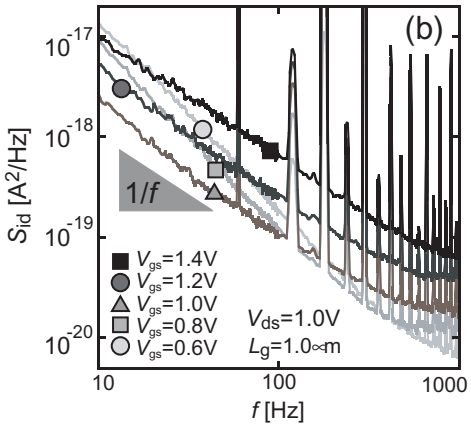
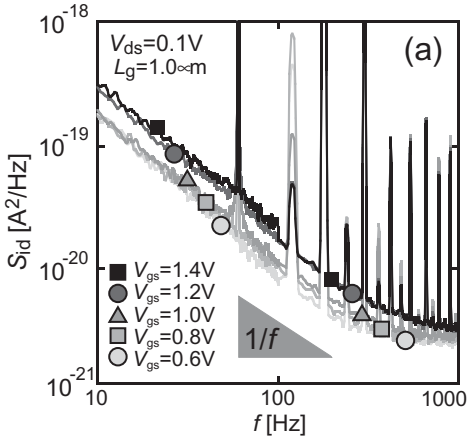


Fig. 6(a) Measured 1/f noise density as a function of frequency for different gate voltages at V_{ds}=0.1V. (b) for V_{ds}=1.0V.

3 1/*f* noise Analysis

Fig. 6a shows measured current noise densities S_{id} as a function of frequency at drain voltage V_{ds}=0.1V for various gate voltage (V_{gs}) values. The measured results provide expected 1/f characteristics for f < 500Hz and reasonably low noise-current densities. However, the case for V_{ds}=1V shows a strongly enhanced 1/f dependence for small V_{gs} values as can be seen in Fig. 6b. Furthermore, the 1/f characteristics are observed only for $V_{gs} > V_{ds}$. Fig. 7 summarizes the measurement results at f=100Hz with symbols as a function of V_{gs} for various V_{ds} values. Similar features as in the bulk case are seen [4].



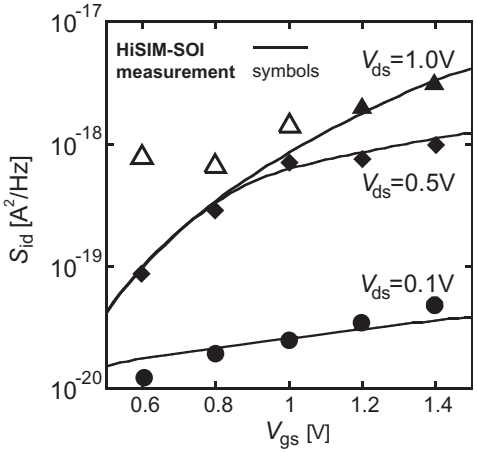


Fig. 7 Calculated 1/f noise density as a function of gate voltage V_{gs} at f=100Hz. Symbols are measurements. Deviation of the three open triangles from the HiSIM-SOI result is attributed to impact ionization, which is not yet included in HiSIM-SOI.

Analysis of the 1/f noise is investigated with the newly developed HiSIM-SOI. The model equation implemented in HiSIM-SOI is

$$S_{\mathrm{id}} = \frac{I_{\mathrm{ds}} \cdot NFTRP}{\beta \cdot f \cdot L_{\mathrm{g}} \cdot W_{\mathrm{g}}} \left\{ \frac{1}{\left(N_0 + N^*\right)\left(N_{\mathrm{L}} - N^*\right)} + \frac{2 \cdot NFALP \cdot \mu}{N_{\mathrm{L}} - N_0} \log\left(\frac{N_{\mathrm{L}} - N^*}{N_0 - N^*} \right) + \left(NFALP \cdot \mu \right)^2 \right\}$$

where the distribution of the carriers along the channel is included explicitly in the carrier concentration N. Simulation results with HiSIM-SOI are depicted by solid lines in Fig. 7. For the HiSIM-SOI simulation two model parameters *NFTRP* and *NFALP* are introduced as usually proposed in [7]. These two parameters are fitted to reproduce measured 1/*f* noise characteristics. The first parameter *NFTRP,* the trap density in the gate oxide, determines the magnitude of the 1/*f* noise; and the second parameter *NFALP*, the noise-current contribution of the mobility fluctuation due to carrier trap/detrap, determines the voltage dependence. It has been observed that nearly the same values of these parameters are obtained, if the technology used for the device fabrication is mature [4]. The fitted *NFTRP* value for the SOI case is slightly different from the bulk-MOSFET. It is expected that the carrier confinement in the SOI-MOSFET plays an important role for the 1/*f* noise characteristics. To clarify this point, detailed investigations must be done for various different devices fabricated independently.

Good agreement of the measured and simulated noise-voltage characteristics is the proof of accurate calculation of the carrier concentration and its distribution along the channel done in HiSIM-SOI. Deviation of three measurement points (open triangles) from simulation results is attributed to impact ionization, called low frequency excess noise by many authors [8, 9]. The model for this effect is not included in our simulation yet.

4 Discussion

To get profit from the carrier confinement in advanced MOSFET devices, technology development tends to use thinner T_{SOI} for achieving better driving capability. Fig. 8 shows predicted noise increase for reduction of T_{SOI} from 50nm to 25nm. Enhancement of the noise density is found to be quite large. This will cause serious problems in real circuit applications. For favorable usage of such advanced devices, it is therefore concluded that a reduction of applied voltages is unavoidable.

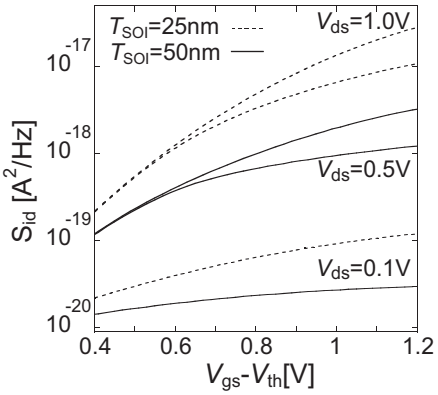


Fig. 8 Comparison of calculated 1/*f* noise for the different SOI-layer thicknesses.

5 Conclusion

We have developed the SOI-MOSFET model HiSIM-SOI. By application of our model we verified that reduction of the silicon layer thickness T_{SOI} enhances the driving capability of the SOI-MOSFET. However, the enhanced noise due to the increased carrier concentration, caused by the inversion-layer confinement, will also cause serious problems in the application of future devices such as the double-gate MOSFET and the FinFET.

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