Compact model for ultra-short channel four-terminal DG MOSFETs for exploring circuit characteristics

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ABSTRACT

A compact model of the DG MOSFETs, which handles two gates independently, is discussed. The model can simulate the DG MOSFETs of asymmetric gate design, together with their four-terminal operation. In this report, we first discuss on the issues concerning to the ultra-short DG MOSFETs and its modeling. Next we present a compact model that includes a mobility modeling as a function of perpendicular and longitudinal electric field. Two approaches are introduced. The results are compared with the device simulator results.

Keywords: MOSFET, double-gate, compact modeling

1 INTRODUCTION

Double-gate field effect transistors (DG MOSFETs), which have two insulating gates sandwiching a Si-channel, as shown in Fig. 1, have gained much attention as the technology node proceeds beyond 100nm. We have proposed a compact model of the DG MOSFETs which handles two gates independently [1]. The model has been improved and has included velocity saturation effect [2]. These models can simulate the DG MOSFETs of asymmetric gate design, together with their four-terminal operation. In this report, we present a model that includes a mobility modeling as a function of perpendicular and longitudinal electric field, and discuss points which are necessary to consider for improving the DG MOSFETs' compact model. And we discuss modeling issues which are specific to DG MOSFETs, compared to the modeling of conventional bulk MOSFETs or SOI MOSFETs.

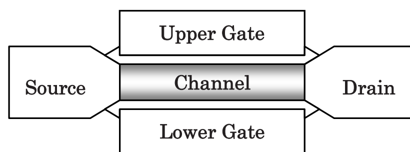

Figure 1: Cross-sectional view of the DG MOSFET

2 MODELING ISSUES

To build a compact model of DG structure necessitates considerations for many aspects that are specific to DG MOSFETs. For example, lack of device data is serious one. Because of this, an empirical model with a number of adjusting parameters confronts difficulty of reasonable parameter extraction. Therefore, a physics-based model with a small set of fitting parameters is more desirable. Also these parameters should have clear default value derived from the discussion based on physics. Apart from such an aspect, there are structure-specific issues as follows.

1) Sandwiched structure

In DG MOSFETs, two gates sandwich a nondoped or lightly doped Si channel. The gates electrically screen the channel region. Electrons are always scattered at two interfaces. When both gates are ON state, there is no inversion electric field or its equivalent. This implies that the tendency of electron confinement at the interface is weaker.

2) Insulated Source/drain structure

Source and drain region may be formed without pn junctions, resulting in much smaller parasitic capacitances. On the other hand, their thickness and the channel thickness will be the same from the process requirements. Gate overlap with the drain region may not be indispensable, again resulting in different capacitance-model approach.

3) Floating body

Partially deplete DG MOSFETs with strong channel-doping behave as two conventional MOSFETs connected in parallel, and they are out of our scope. In the case of undoped-channel DG MOSFETs, whenever the parasitic bipolar transistor plays some role, it becomes uncontrollable. For very-short channel DG MOSFETs, operation voltage smaller than silicon bandgap is significant.

These aspects call for consideration on following issues.

2.1 Mobility model

In BSIM3 or BSIM4, there are three or four mobility models. Those all have style of empirical formula. In HiSIM, the mobility model resembles physics-based models adopted in device simulators like ATLAS. In the compact model for DG MOSFETs, it is desirable that the mobility model is simple and physics-based. From this respect, CVT model in the ATLAS device simulator is adequate. But the model predicts very low mobility when the channel doping is set to be zero. We formulated a mobility model, starting from the bulk mobility, simulating the universal curve, adding roughness scattering inversely proportional to the channel thickness which is always present in the case of DG MOSFETs. The model that we developed will be described in the next section.

2.2 Short-channel effect

Since the drain electric field in the channel decays exponentially, DIBL is expected to be very small. The drain potential-field penetrating into the channel can be expressed as $A\exp(\pi(x-L_G)/\lambda)$, where L_G is the gate length, and λ is the characteristic length approximately equal to the sum of thickness of the channel and the two gate oxides. When the dielectric constant of the oxide is lower (higher) than the channel dielectric constant, λ is longer (shorter) than the above-mentioned total thickness. The DIBL becomes significant only when 2λ is comparable to L_G. Since λ for typical DG MOSFETs will below 50nm, short channel effect at large drain voltage is always accompanied by carrier velocity-saturation effect that limits current enhancement. Output conductance at the saturation region will be small even in ultra-short channel MOSFETs.

2.3 Quantum effect

Quantum size-effect will set in for the channel as thin as 5nm. Although it causes V_{th} increase, the amount is small (<10mV). More prominent effect is higher mobility by the band splitting. For thin channel, band fluctuation caused by channel-thickness fluctuation is also significant. Its modeling will be process dependent.

3 MODEL

3.1 Mobility modeling

We adopt mobility model that resembles universal curve. The perpendicular electric field at the interface E_{tr} is the variable. The mobility is described as

$$\mu^{-1} = \mu_0^{-1} + \mu_{PH}^{-1} + \mu_{SR}^{-1} \tag{1}$$

where μ_0 is the bulk mobility, μ_{PH} is the contribution by the phonon scattering, μ_{SR} is the contribution by the interface roughness. In practical, μ_{PH} is treated as the term which describes $E^{-1/3}$ rule region of the universal curve:

$$\mu_{PH} = 5.85\times10^4 \times E_{tr}^{-1/3}\,. \tag{2}$$

Since acoustic phonon scattering term in CVT model is related to the channel doping, it is questionable that DG MOSFETs with no channel doping have the mobility that obeys the universal curve. Detailed comparison with real devices will resolve this issue.

Also the mobility μ_{SR} does not necessarily mean contribution by the surface roughness scattering, and is treated as the term which describes E^{-2} dependency:

$$\mu_{SR} = 4\times10^{15}\left(E_{tr} + kT/qT_{Si}\right)^{-2}, \tag{3}$$

where kT is the thermal energy, T_{Si} is the channel thickness. The additional term kT/qT_{si} is added to describe surface scattering caused by the quantum-well structure of the channel.

Rigorously speaking, the transport equation should be solved by treating the mobility as a variable, since E_{tr} varies inside the channel. But this approach is time-consuming, since the equation is analytically unsolvable. Therefore it cannot be adopted as a compact modeling. Instead, we approximate that the mobility derived by eq. (1) is constant in the entire channel. We also assumed that the value is equal to that at the source end.

3.2 Velocity saturation modeling

At high longitudinal electric field, carrier velocity saturates. This can be expressed as the decrease of the carrier mobility such as

$$\mu \to \left(1 + \left|E/E_c\right|^2\right)^{-1/2}\mu\,, \tag{4}$$

where E_c is the critical electric field that describe the velocity saturation. Since E varies inside the channel, it adds another variable terms to the transport equation. In conventional compact models such as BSIM and HiSIM, the prefactor of the expression (4) is treated to be constant in the entire channel. This approach is attractive because the transport equation remains identical. On the other hand, this approach substitutes 'velocity saturation' to 'mobility degradation,' changing the physics behind the model. We call it here the constant-μ integration (μ_{cons}) approach.

To treat the velocity saturation rigorously, substitution (4) should be performed to the transport equation as

$$-q\mu\left(\frac{q}{C}\frac{dn}{dy}n + \frac{kT}{q}\frac{dn}{dy}\right) = I_D\left(1 + \left|\frac{E}{E_c}\right|^2\right)^{1/2}, \tag{5}$$

where μ is the low-field mobility, n is the carrier density in

the channel, C is the effective capacitance for the channel, I_D is the drain current. We call it here the variable-μ integration (μ_{var}) approach.

The equation is solved as

$$-\beta E_c n_b L_{eff} = \frac{1}{2}\left(n_{aL}\sqrt{n_{aL}^2 - n_b^2} - n_{a0}\sqrt{n_{a0}^2 - n_b^2}\right) - \frac{1}{2}n_b^2 \log\left(\frac{n_{aL} + \sqrt{n_{aL}^2 - n_b^2}}{n_{a0} + \sqrt{n_{a0}^2 - n_b^2}}\right), \quad (6)$$

where L_{eff} is effective channel length, and

$n_{aL}=n_a(L_{eff})$,
$n_{a0}=n_a(0)$,
$n_a = n/\left(CkT/q^2\right)+1$,
$n_b = \left(I_D/q\mu E_c\right)/\left(CkT/q^2\right)$.

In this approach, iteration is necessary to obtain drain current, causing slowdown of the computational speed.

3.3 Pinch-off point

In the μ_{var} approach, it becomes impossible to apply Brews' equation

$$V_D = \psi_s(L) - \psi_s(0) + \frac{1}{\beta}\ln\frac{n(0)}{n(L)}, \quad (7)$$

for the drain-end boundary condition, since the lowest carrier density at the drain-end is limited. Instead we apply the condition for the pinch-off point:

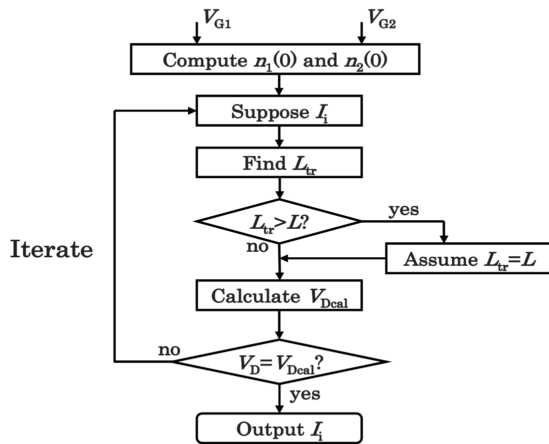

Figure 2: Algorithm for the variable-μ integration (μ_{var}) approach

$$\frac{d^2n}{dy^2}\bigg/\frac{dn}{dy} = \frac{1}{\lambda}, \quad (8)$$

which means that, at the point, surface potential caused by the carrier density change will be connected most smoothly to the surface potential caused by the infiltration of the drain electric field. Before this point we assume that the surface potential is determined only by the carrier density change, and after this point we assume that the potential is determined by the drain electric field. The advantage of this approach is that we can determine the pinch-off point without any fitting parameter.

In the case of the μ_{cons} approach, we have to determine pinch-off point by setting several fitting parameter, causing the model less physics-based. In the next section, the μ_{cons} approach without effective gate length modulation is shown.

Fig. 2 shows the computational algorithm of the model by the μ_{var} approach.

4 RESULTS AND DISCUSSION

DG MOSFETs of a thin silicon channel (T_{si}=10nm) is tested both by the compact model with two approaches and the ATLAS simulator. Two gate oxides have the same thickness (2nm). For ATLAS simulator, CVT model with default values is used as the mobility model. Channel doping of 10^{14}/cm^3 is assumed only to obtain simulation stability. To exclude source and drain resistance, highly doped (10^{21}/cm^3), and extremely short (2nm) source and drain region is supposed. For the compact model, only saturation velocity v_{sat} is changed between these two approaches of the compact model: v_{sat} for μ_{var}(μ_{cons}) is set to be 1.15x10^7 (0.66x10^7) cm/s.

In Fig. 3, simulation results of 50nm and 200nm long DG MOSFETs are shown. For the μ_{cons} approach, discrepancy with ATLAS results is noticeable even for the 200nm long device. And for the 50nm long device, saturation current is much lower than that of ATLAS results. In contrast to this, good agreement is obtained for the μ_{var} approach, both for the 200nm long and 50 nm long devices.

This feature is more prominent when we compare the output conductance as shown in Fig. 4, where the μ_{var} approach shows excellent agreement with the ATLAS results in the saturation region, while the μ_{cons} approach fails completely.

As expected, short channel effect of DG MOSFETs is small as far as the channel length is much longer than the channel thickness, as shown in Fig.4. Still the short channel effect may become large when the ratio of the gate length to the channel thickness approaches 2. In Fig. 5, results for a 20nm DG MOSFET are shown. Even in such a short channel, current does not increase drastically. It is not because the short channel effect is weak. As shown in the same figure, source-ward shift of the pinch-off point is drastic. Therefore the reason why the output conductance is low is that carrier velocity saturates and cannot increase

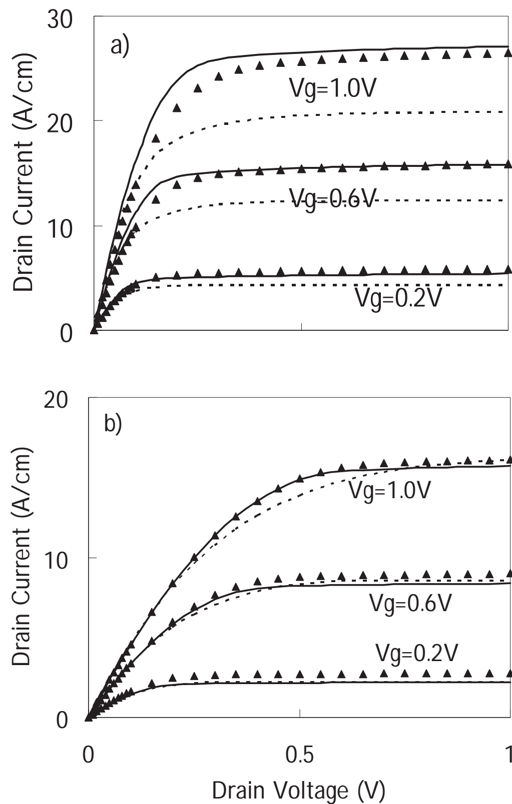

Figure 3: I-V characteristics of 50nm-long (a) and 200nm-long (b) devices, by the μ_{var} approach (solid lines), the μ_{cons} approach (dashed lines) and the ATLAS device simulator (triangles).

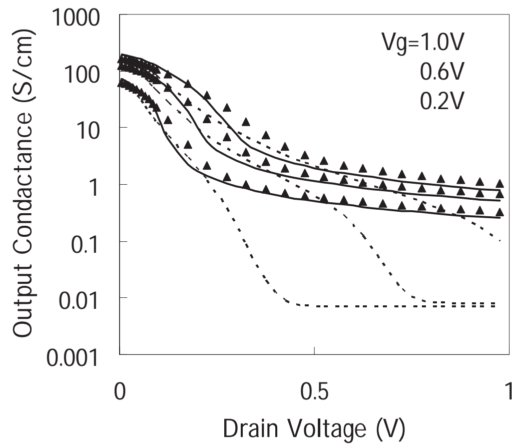

Figure 4: Output conductance of a 50nm-long device, by the μ_{var} approach (solid lines), the μ_{cons} approach (dashed lines) and the ATLAS device simulator (triangles).

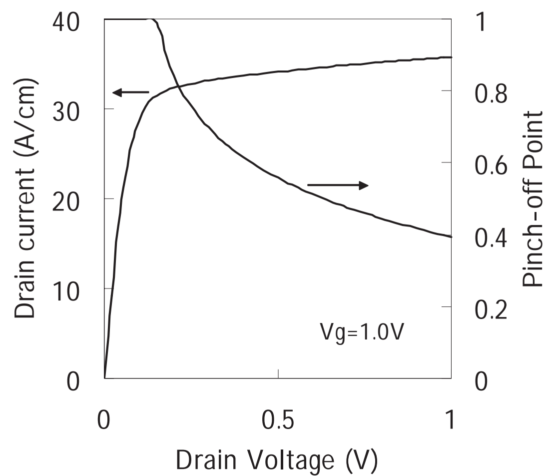

Figure 5: Drain current and the pinch-off point for a 20nm-long DG MOSFET.

anymore. It also implies that the simulation result is not so sensitive to the determination of the pinch-ff point. It explains why the crude assumption of eq. (8) works very well.

5 SUMMARY

We discussed issues for constructing a compact model of ultra-short channel DG MOSFETs. We proposed a compact model of the DG MOSFETs with mobility modeling, starting from the bulk mobility, modulating according to the universal curve, adding roughness scattering inversely proportional to the channel thickness. Two approaches were compared to handle the carrier velocity saturation. These results are compared each other, and with the device simulator results. Better agreement with device simulator was obtained when the velocity saturation effect is included as a variable in the transport equation.

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