HiSIM-1.2: The Effective Gate Geometry Determination with the Capacitance Data

Y. Jino

Silvaco Japan 549-2 Shinano-machi Totsuka-ku, Yokohama, Japan, yoshihisa.iino@silvaco.com

ABSTRACT

This paper describes an effective MOS gate geometry determination of HiSIM (Hiroshima-university STARC IGFET Model) [1, 2] using the gate capacitance data. Although the method is quite straight forward, the step shouldn't be neglected. Since the calculated charges based on the surface potential are commonly used for both the current-voltage and the capacitance-voltage characteristics, no dedicated parameters are required for the gate capacitance of HiSIM. Therefore, the capacitance data validation might be overlooked with the good fitting results of the current-voltage curves. However, the gate capacitance values could deviate from the actual devices when the improper gate geometry would be defined, which is practicaly dangerous. The HiSIM gate capacitance which are derived from the gate charges, are the function of the gate dimension.

Keywords: HiSIM, surface potential, parameter extraction, compact model, effective channel length

1 INTRODUCTION

HiSIM-1.2 model parameter extraction and the resulted fit for the current voltage characteristics were reported at WCM-2004 [3]. The measurement curves were reproduced well. However, the Cgc (the gate to the shorted source/drain) capacitance simulations were found later to have the large discrepancy for the short channel length devices in spite of the good fit for the large one: Figure-3. The author who had been nurtured as a traditional compact model engineer had little consideration, although he tried, on the nature of HiSIM: the HiSIM capacitance as the gate charge derivative naturally depends on the MOS gate geometry. A length correction parameter for the effective channel length calculation clearly solved the disagreement. Despite the measure is simple, the significance shouldn't be overlooked. HiSIM effective geometry has to be extracted using the gate capacitance data. The good fit on the DC curves does not guarantee the HiSIM capacitance behavior when the improper geometry is defined.

2 MEASUREMENT DATA

2.1 Geometry Selection

The geometry selection for the gate capacitance measurement is the same as for the parameter extraction using the current-voltage characteristics: Large, L-array, and W-array devices. The short and the narrow channel sizes are limited due to the very small capacitance values.

The prepared device data were N-channel devices as following.

Large device: the channel width and length were 10 um. L-array devices: the fixed channel width was 10 um and the channel lengths were 5.0, 1.0, 0.5, 0.3 and 0.2 um.

2.2 Measurement Conditions and the Results

Agilent 4284 LCR meter was used. And the gate terminal DC bias was swept from 0 to 1.2 volts with the shorted source and the drain terminals connected to the ground. Also, the bulk voltage was stepped.

Figure 1 and 2 are the measured capacitance characteristics for the L-array devices normalized to the L=10um and L=1um, respectively. The peak capacitance values are almost proportional to the channel lengths for L=10, 5, and 1um, and slightly deviated from the proportionality for the shorter channel length devices.

Figure 3 is for the measurement versus HiSIM-1.2 model simulations. The model parameters used were extracted just for the current-voltage characteristics, and the capacitance characteristics were verified only for the large device. The clear discrepancy of the simulation is observed at the channel length of 1um, and below.

Figure 4 shows the improved simulation curves with the adjusted HiSIM-1.2 geometry parameters, and the fitting is pretty good.

3 CONCLUSION

On the extraction of HiSIM model parameters, the capacitance-voltage characteristics for rather short channel devices must be used to adjust the geometry correction parameters of HiSIM.

4 ACKNOWLEDGEMENT

The author would like to thank Semiconductor Technology Academic Research Center for the measurement and the permission to use the practical device data.

REFERENCES

- [1] M. Miura-Mattausch, et al., "HiSIM: A MOSFET Model for Circuit Simulation Connecting Circuit Performance with Technology," Tech. Digest IEDM, pp. 109-112, 2002.
- [2] Semiconductor Technology Academic Research Center
 - http://www.starc.or.jp/kaihatu/pdgr/hisim/index.html
- [3] Y.Iino, "A Trial Report: HiSIM-1.2 Parameter Extraction for 90nm Technology," 2004 Workshop on Compact Modeling, 2004 NSTI Nanotechnology Conference & Trade Show, Boston, Massachusetts, U.S.A. http://www.nsti.org
- [4] HiSIM1.2.0 User's manual: http://www.starc.or.jp/kaihatu/pdgr/hisim/index.html

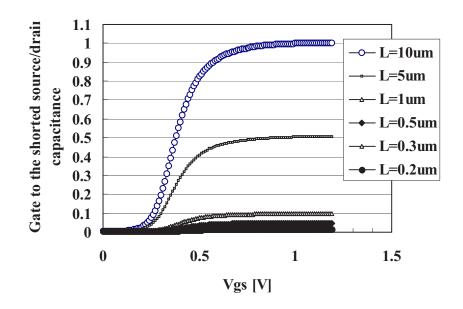


Figure 1:Normalized Capacitance for L = 10um

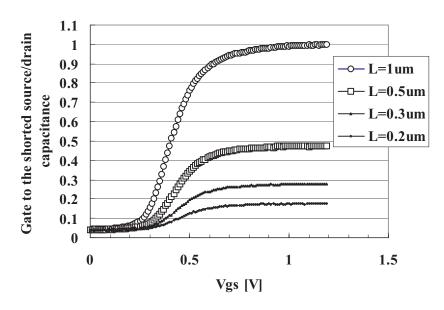


Figure 2:Normalized Capacitance for L = 1um NSTI-Nanotech 2005, www.nsti.org. ISBN 0-7/67985-3-0 WCM, 2005

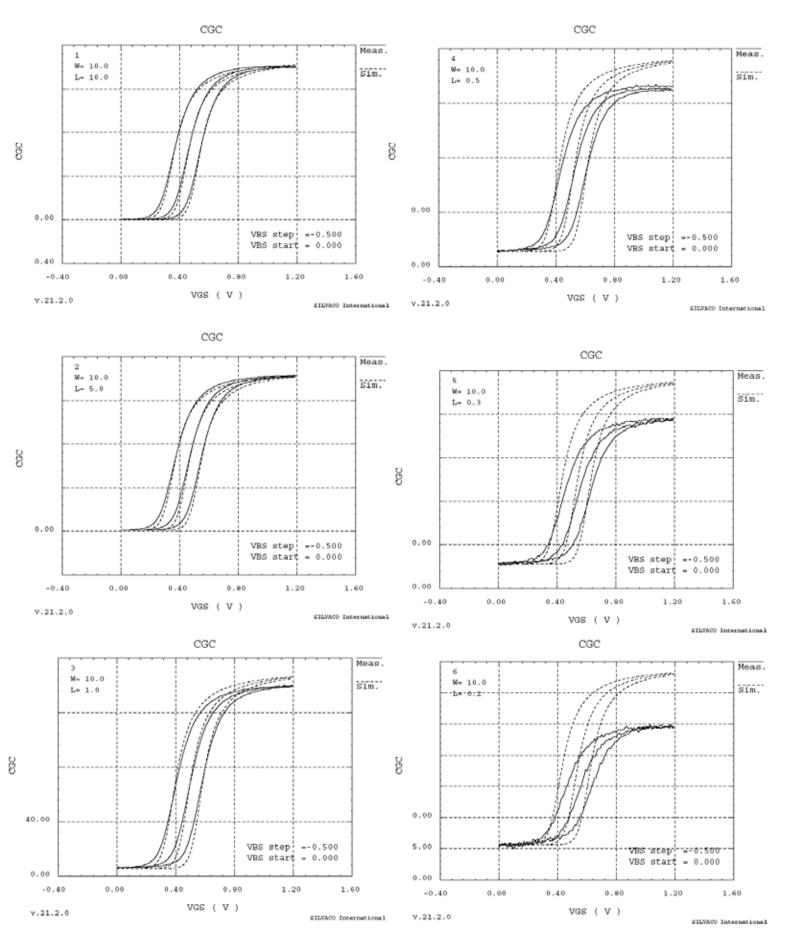


Figure 3: Capacitance-Voltage Characteristics HiSIM-1.2 model with no geometry correction

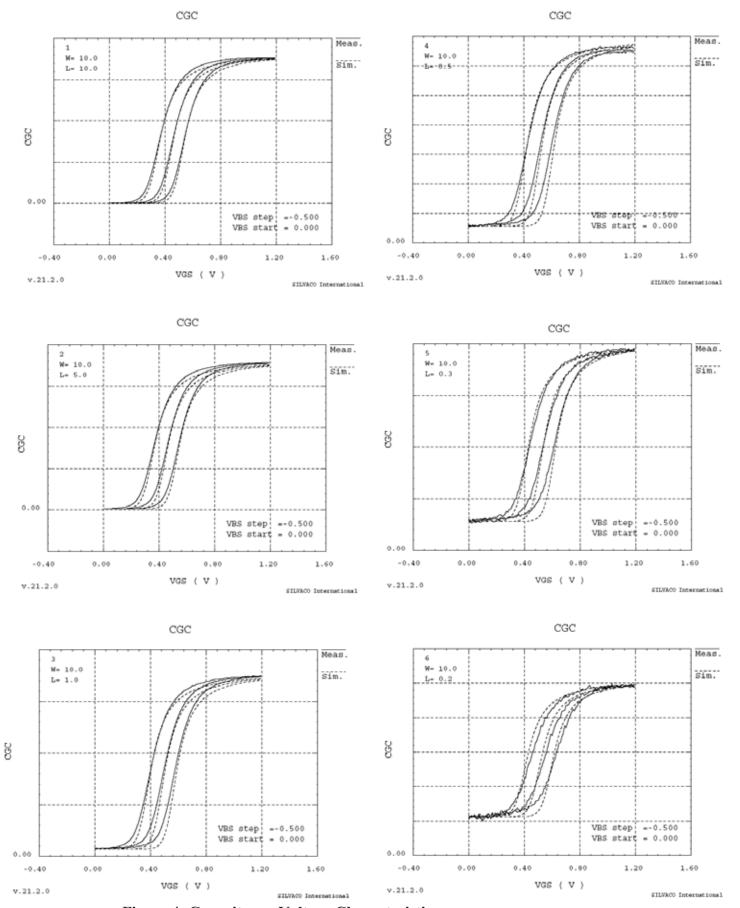


Figure 4: Capacitance-Voltage Characteristics HiSIM-1.2 model with the geometry correction