HiSIM: Accurate Charge Modeling Important for RF Era

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ABSTRACT

Extension of the gradual-channel approximation is presented with the surface-potential-based MOSFET modeling. All phenomena observed under the saturation condition are described by the potential increase in the pinch-off region in a self-consistent way. The charge induced by the high lateral electric field is demonstrated to become a major contributing factor in the charge distribution of small-size MOSFETs, instead of the conventional intrinsic part. This changes the charge partitioning of the inversion charge, which changes the high frequency response of small-size MOSFETs as well.

Keywords: MOSFET Model, Surface Potential, Charge-Based Modeling, Sub-100nm Technology

1 INTRODUCTION

Small-size MOSFETs are key for RF applications [1]. Further improvement of high frequency characteristics is undertaken to meet aggressive requirements. For utilizing the improvement and achieving reliable design of RF circuits, accurate modeling of small-size MOSFET characteristics is indispensable [2]. Till now the gradual-channel approximation is adopted to derive analytical equations for describing device performances. However, conventional modeling concepts cannot be extended to realize accurate description for such devices. The reason is that the lateral electric field along the MOSFET channel is becoming more pronounced in small-size MOSFETs, weakening the V_{gs} control, and thus diminishing the MOSFET feature. Though investigations [3] have been undertaken to solve this problem, they exclude the pinch-off region itself, where the high electric field occurs. We demonstrate here that the inclusion of the charge in the pinch-off region is important to simulate accurate MOSFET performances. Thus an extension of the gradual-channel approximation is the task that we investigate here.

2 Device Characteristics under the Saturation Condition

Fig. 1 shows a comparison of measured g_{ds} between a long-channel and a short-channel MOSFET [4]. The large g_{ds} value of the short-channel MOSFET under the saturation condition is modeled as the channel-length modulation [5]. The concept is based on the argument that the velocity reaches its maximum value to compensate the reduction of carrier density in the pinch-off region. Fig. 2 shows the same comparison but for C_{gd}. Under the saturation condition the overlap capacitance C_{ov} and the lateral-field-induced capacitance C_{Q_y} are important components in the C_{gd} value as can be seen schematically in Fig. 3 [6].

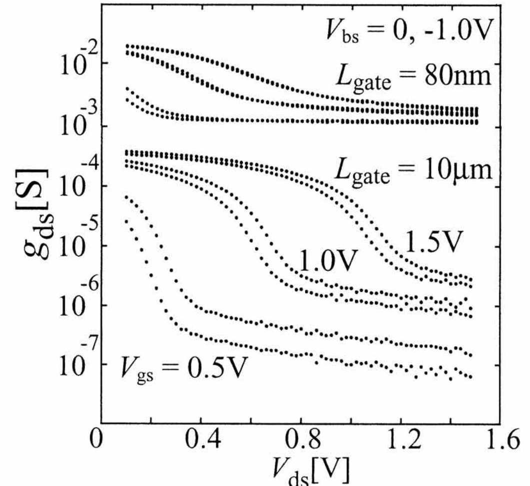

Figure 1: Measured channel conductance g_{ds} for two gate lengths.

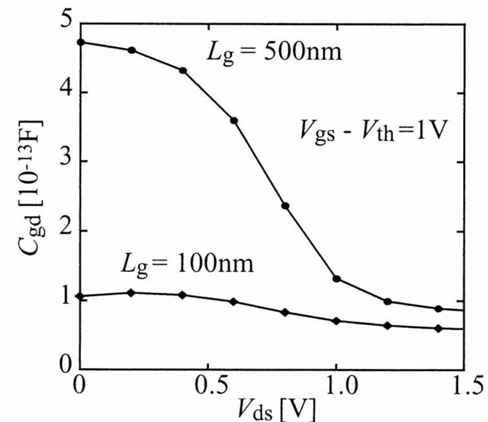

Figure 2: Measured gate-drain capacitance C_{gd} for two gate lengths.

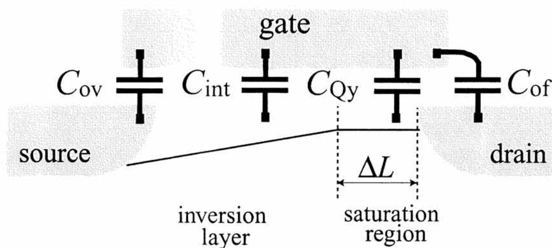

Figure 3: Gate-drain capacitance components at saturation where the overlap and lateral-field-induced capacitances dominate.

Y-parameter ($Y_{\rm gg}$ and $Y_{\rm gd}$) calculations are shown in Figs. 4a and b for with and without the gate resistance $R_{\rm g}$. Calculations are carried out under the saturation condition [7], [8]. It is seen that the $R_{\rm g}$ contribution is drastic. However, in the intrinsic contribution of Y-parameter capacitances play important role as demonstrated by thick lines. Among the capacitances, $C_{\rm ov}$ and C_{Q_y} dominate at saturation condition, where most circuits are operated. These capacitances are determined by charges stored around the drain (see Fig. 3).

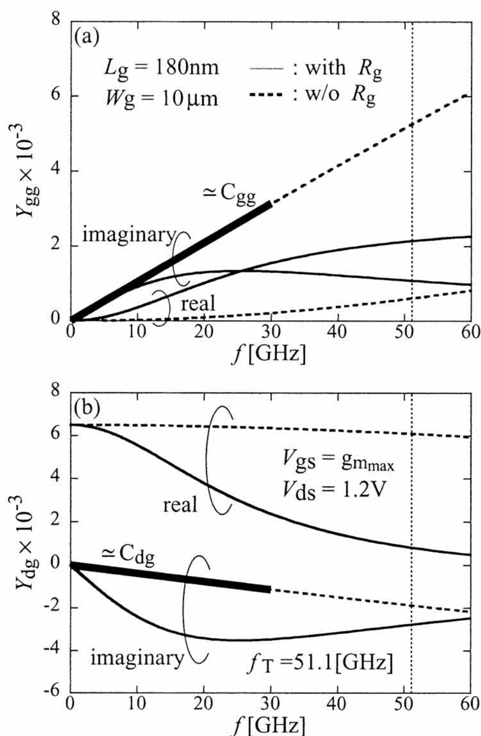

Figure 4: Comparison of calculated n-MOSFET Y-parameters for with and without the gate resistance $R_{\rm g}$. Thick lines indicate calculated capacitances.

3 Charge Description

We have demonstrated that a charge-based model with the self-consistent surface-potential description offers a basis for successfully modeling observed phenomena [4], [9]. HiSIM (Hiroshima-university STARC IGFET Model) is developed according to this concept [10], [11], solving the Poisson equation and the current-density equation including both the drift and the diffusion contributions analytically. Here two additional approximations are adopted: the charge-sheet approximation and the gradual-channel approximation. These approximations allow analytical formulations describing device performances as functions of the surface potentials at the source side $\phi_{\rm S0}$ and at the drain side $\phi_{\rm SL}$ [12], [13]. These potentials are calculated by solving the Poisson equation iteratively. The enhancement of the simulation time is suppressed by developing good initial values for the iteration. The surface potentials are shown in Figs. 5a and b. It is seen that $\phi_{\rm SL}$ never reaches $V_{\rm ds}$. Fig. 6 compares the surface potential calculated analytically and the exact solution with a 2D device simulator. The $\phi_{\rm SL}$ value obtained analytically is the value at the end of the gradual-channel approximation.

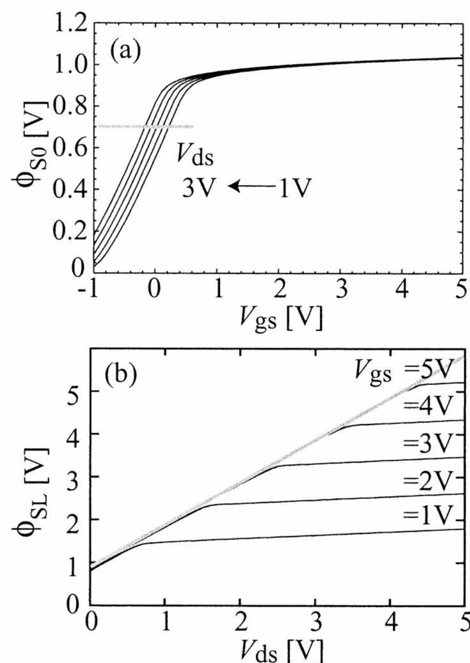

Figure 5: Calculated surface potential values with HiSIM.

Origin of the charges is the surface potential along the channel induced by applied biases. However, the distribution of the surface potential cannot be known analytically. We approximate the distribution with a simple function of position in the channel as shown schematically in Fig. 7. The model parameters are dependent on the channel/contact impurity profile. The potential value $\phi_{\rm S}(\Delta L)$ determines the value at the metallurgic junction. The steep potential increase in the pinch-off region causes a high lateral electric field, inducing charges in the saturation region as demonstrated in Fig. 8 [6]. The position where the field maximum occurs is defined

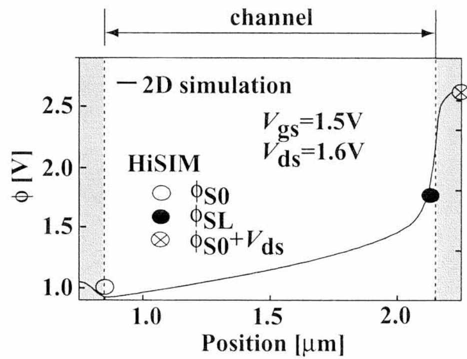

Figure 6: Simulated surface-potential distribution along the channel with a 2D simulator MEDICI.

by a model parameter x_{Q_y}. The space charge Q_y induced by the lateral electric field is calculated by applying the Gauss law in the pinch-off region. The capacitance C_{Q_y} due to this charge is given by $C_{Q_y} = \mathrm{d}Q_y/\mathrm{d}V$, and is added to the conventional intrinsic $C_{\rm gd}$ components as shown in Fig. 9. Here the potential increase is dependent on the channel/drain junction, which determines the channel length modulation as well [14]. The length of the pinch-off region is modeled a function of $\phi_{\rm S}(\Delta L)$.

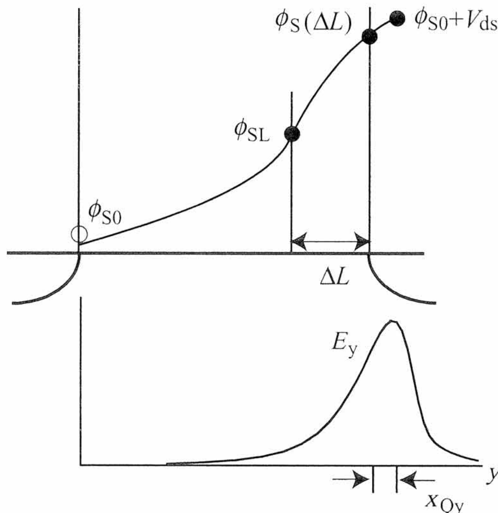

Figure 7: Schematic representation of the surface potential distribution along the channel. The lateral field resulting from the steep potential increase near the drain region is also depicted.

3.1 Accurate Charge Partitioning Description

All device characteristics are described by the surface potential values. The surface potential based description allows dynamic partitioning of the inversion charge $Q_{\rm I}$. The lateral-field-induced charge is included in $Q_{\rm D}$. Partitioned charges $Q_{\rm S}$ and $Q_{\rm D}$ are shown in Figs. 10 and 11 for a long-channel case and a short-channel case,

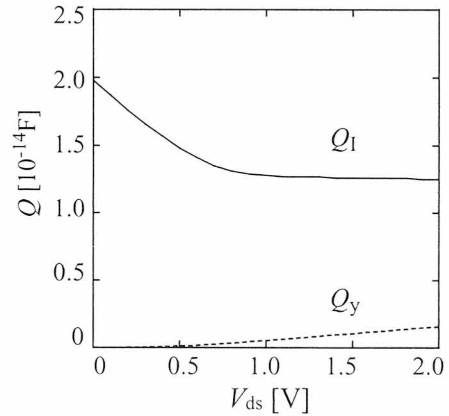

Figure 8: Calculated charges as a function of the drain-source bias $V_{\rm ds}$. The Q_y contribution becomes significant at saturation condition.

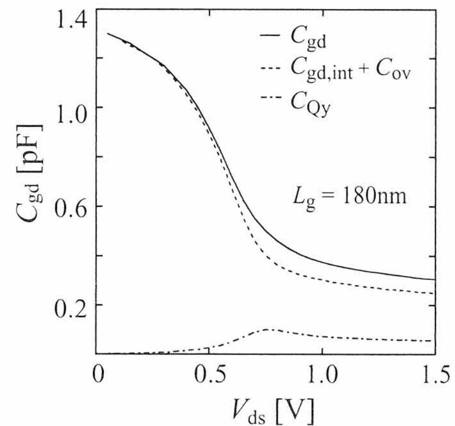

Figure 9: 2D simulation result of $C_{\rm gd}$ components: the intrinsic capacitance $C_{\rm gd,int}$, the overlap capacitance $C_{\rm ov}$, and the lateral-field-induced capacitance C_{Q_y}.

respectively. Smooth transition from 50/50 to 60/40 is seen for the long-channel case. However, the Q_y contribution modifies the ratio in the saturation region for the short-channel case. This modification results from an accurate description of the charges within the channel and proves to be significant for modeling of small-size MOSFETs. Charges in the overlap region at the source/drain are calculated directly from the known surface potential values, $\phi_{\rm S}(\Delta L)$ and $\phi_{\rm S0} + V_{\rm ds}$, as shown in Fig. 7. Calculated $C_{\rm gd}$ for different gate lengths are compared with measurements in Fig. 12.

4 CONCLUSION

We demonstrated a model including the lateral-electric-field contribution for simulating MOSFET characteristics under the saturation condition in a self-consistent way. With this model all phenomena observed in the saturation condition are calculated accurately. This model secures correct simulation for the 100nm-MOSFET generation and beyond.

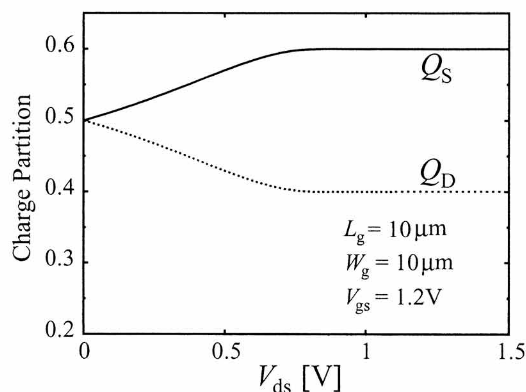

Figure 10: Charge partitioning ratio of calculated charges for $L_g = 10\mu m$. 60/40 is seen at saturation condition.

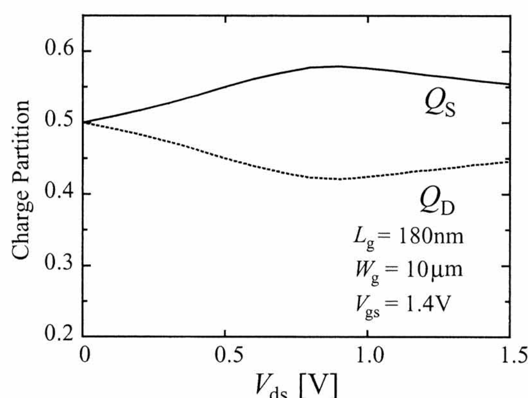

Figure 11: Changes in the charge partitioning ratio upon inclusion of the lateral-field-induced charge to Q_D. This is well-observed in small-size MOSFETs.

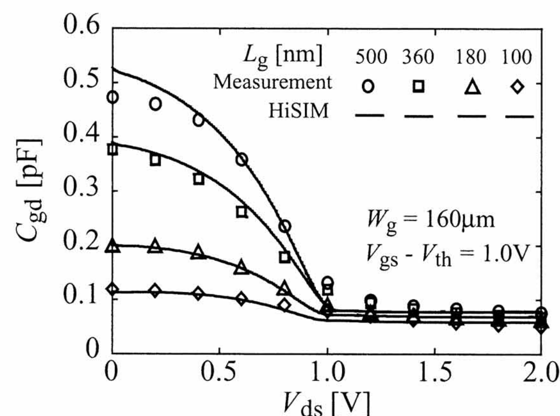

Figure 12: HiSIM calculation of C_{gd} for different gate lengths. In this calculation, the overlap and lateral field components are included.

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