

Recent enhancements of MOS Model 11

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ABSTRACT

MOS Model 11 (MM11) is a surface-potential-based compact MOSFET model, which was introduced in 2001 (level 1100). An update of MM11, level 1101, was introduced in 2002. At the moment a second update of MM11, level 1102, has been completed and is under test. It includes: *i*) an iterative solution of the surface potential; *ii*) an improved description of the velocity saturation yielding a better modelling of the transconductance in saturation; and *iii*) a better description of noise, especially the induced gate current noise. In this paper we describe these improvements and show the resulting improved modelling of transistor performance.

Keywords: MOS Model 11, compact MOSFET modelling, surface potential, thermal noise, induced gate noise

1 INTRODUCTION

There are three categories of compact MOS models: *i*) threshold-voltage-based models, *ii*) inversion-charge-based models, and *iii*) surface-potential-based models. Since the latter category of models give a physics-based and accurate description in all operation regions, experts judge them to be the most successful in describing deep-submicron CMOS technologies for demanding analogue and RF applications [1]. As a result, most new MOS models in the public domain are surface-potential-based [1]–[3].

MOS Model 11 (MM11) is a surface-potential-based compact MOSFET model, which has been developed with special emphasis on the preservation of source-drain symmetry and on an accurate description of distortion behaviour. MM11 was introduced in 2001 (level 1100, indicated by MM1100) and contains all major physical effects such as poly-depletion for the gate, gate tunnelling current and quantum-mechanical quantisation effects. During 2002, an update of MM11, level 1101 (MM1101), has been introduced [4]. The main enhancements of MM1101 over MM1100 are: *i*) the modelling of gate-induced drain leakage, *ii*) a rigorous separation of geometrical and temperature scaling rules for the model parameters, and *iii*) a separate set of geometrical scaling rules for the model parameters, especially designed

for binning. In MM1101, there is a choice to use the physics-based geometrical scaling rules **or** the binning geometrical scaling rules for the model parameters.

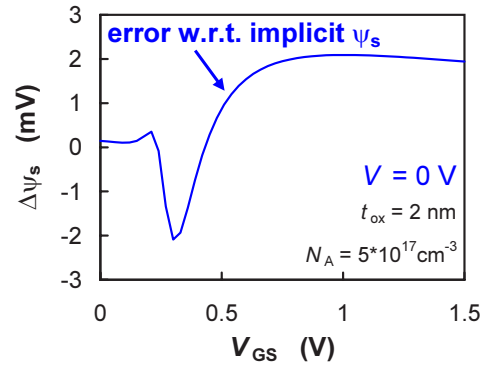


Figure 1: Absolute error in the approximate surface potential (as used in MM1101) with respect to the exact solution of the implicit equation.

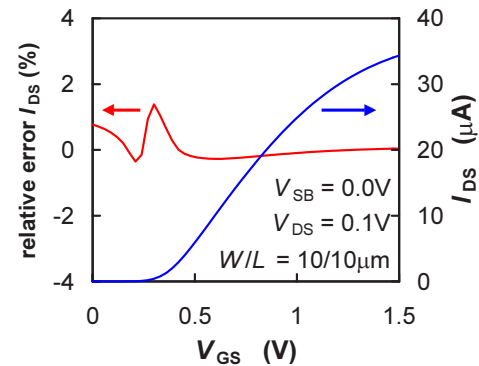


Figure 2: Relative error in the current using the approximated and exact solution of the surface potential corresponding to Fig. 1.

As mentioned before, surface-potential-based models give a physics-based and accurate description in all operation regions. The main drawback of these models, however, is the fact that only an implicit equation for the surface potential can be derived. The solution to this implicit equation can be either approximated an-

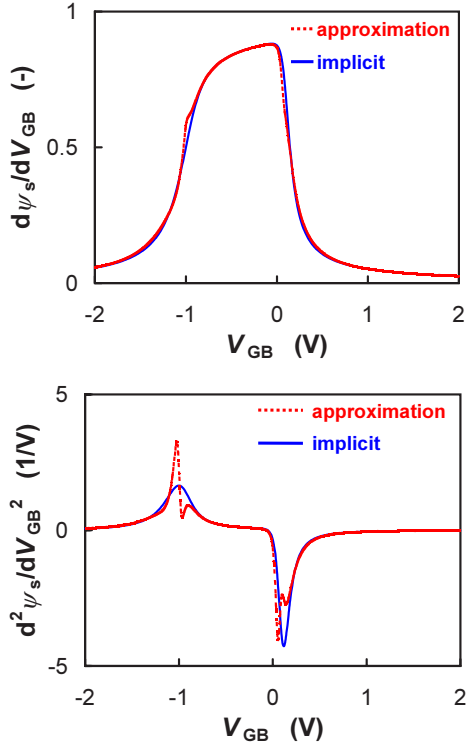


Figure 3: First-order derivative (**top**) and second-order derivative (**bottom**) of the surface potential ψ_s with respect to the gate-bulk voltage. Both the result of the implicit relation for surface potential (*solid line*) and the explicit approximation for surface potential as used in MM1101 (*dashed line*) are shown.

alytically or found exactly by iteration. MM1101 uses an analytical approximated solution of the surface potential, which is computationally very efficient [5]. This approximated solution shows only small deviations with respect to the exact solution of the implicit equation for the surface potential, see Figure 1. The error in the current caused by this deviation is negligible, see Figure 2. When, however, the first-order and, especially, the second-order derivatives of the surface potential with respect to the gate-bulk voltage are inspected, larger deviations show up, see Figure 3. This leads to an error in the input capacitance C_{GG} , and may be a problem when modelling the distortion of MOS varactors.

More accurate analytical approximations for the surface potential have been published [1], [6]. These approximations are, however, also computationally inefficient compared to our approximation. Therefore we have adopted an iterative solution of the surface potential in MM1102. In addition to this we have also improved the description of the velocity saturation and added a better description of noise, especially the induced gate current noise. These three improvements

will be described in the next Sections.

2 ITERATIVE SOLUTION OF THE SURFACE POTENTIAL

The surface potential ψ_s is defined as the electrostatic potential at the gate oxide/substrate interface with respect to the neutral bulk. For an n -type MOSFET with uniform substrate doping N_A and oxide capacitance C_{ox} , ψ_s can be calculated from the following implicit relation [7]:

$$\left(\frac{V_{GB}^* - \psi_p - \psi_s}{k_0}\right)^2 = \psi_s + \phi_T \cdot \left[\exp\left(-\frac{\psi_s}{\phi_T}\right) - 1\right] \quad (1)$$

$$+ \phi_T \cdot \exp\left(-\frac{\phi_B + V}{\phi_T}\right) \cdot \left[\exp\left(\frac{\psi_s}{\phi_T}\right) - \frac{\psi_s}{\phi_T} - 1\right]$$

where V_{GB}^* is the effective gate bias ($V_{GB}^* = V_{GB} - V_{FB}$), V_{FB} is the flat-band voltage, ψ_p is the potential drop in the polysilicon gate due to poly-depletion, k_0 is the body factor of the silicon substrate ($k_0 = \sqrt{2} \cdot q \cdot \epsilon_{Si} \cdot N_A / C_{ox}$), ϕ_T is the thermal voltage ($\phi_T = k \cdot T / q$), and ϕ_B is twice the intrinsic Fermi-potential ($\phi_B = 2 \cdot \phi_T \cdot \ln(N_A / n_i)$). The above implicit relation for ψ_s can be solved iteratively using the Newton-Raphson method [8]. Using a simple yet accurate zero-order estimate of ψ_s and applying a first-order Newton-Raphson scheme to the implicit equation for the surface potential, a maximum of four iterations is needed to reach an accuracy of $10^{-10} \cdot \phi_T$, where ϕ_T is the thermal voltage, see Figure 4. In an attempt to reduce the number of iterations needed to reach this accuracy, a second-order Newton-Raphson scheme has been investigated, see Figure 5. From this figure it can be seen that a maximum of only three iterations is needed to reach the same accuracy. Although the computational effort per iteration is slightly larger for the second-order Newton-Raphson scheme compared to the first-order Newton-Raphson scheme, the overall computation time is smaller for the second-order Newton-Raphson scheme. Hence we adopted the second-order Newton-Raphson scheme for MM1102. In Figure 6 the third-order derivative of the surface potential is shown as a function of gate-bulk voltage. From this figure it can be seen that with MM1102, the distortion modelling of varactors is greatly improved.

3 IMPROVED DESCRIPTION OF VELOCITY SATURATION

Although MM1101 gives an accurate description of the output I_D - V_{DS} characteristics of short-channel devices, it nevertheless gives a slightly inaccurate description of transconductance g_m in the saturation region, see Figure 7 (top). Close examination shows that this

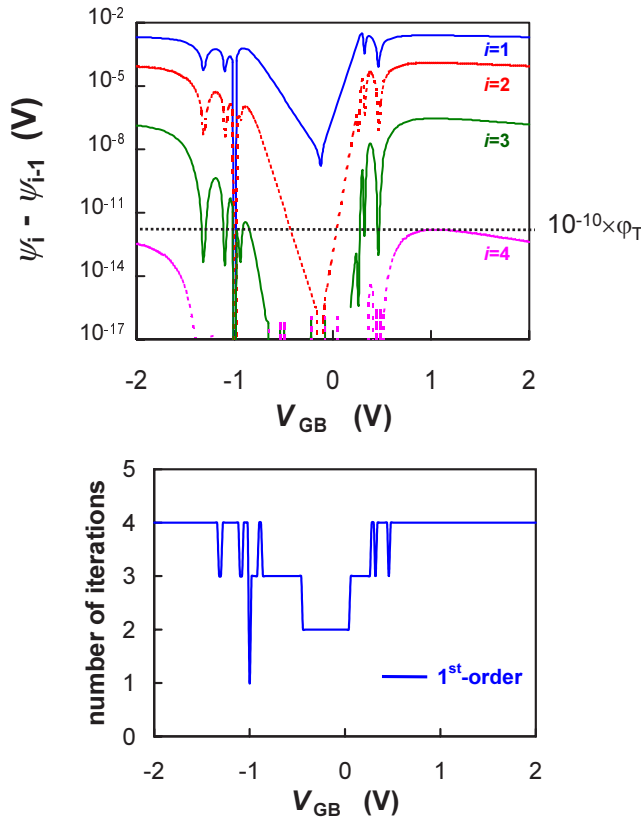


Figure 4: **Top:** Absolute error in surface potential (as a function of gate-bulk voltage) between two successive iterations, where the number of 1st-order Newton-Raphson iterations is indicated by i . **Bottom:** Number of iterations that is needed to obtain an absolute error in surface potential between two successive iterations smaller than 10^{-10} times the thermal voltage.

inaccuracy is caused by the velocity saturation expression used in MM1101. In MM1102, therefore, a more physical and accurate expression for velocity saturation is introduced, see Figure 7 (bottom). In this Section, we will briefly describe the derivation of this new velocity saturation expression.

With an increase in lateral electric field, carriers gain sufficient energy to be scattered by optical phonons, resulting in a decrease of mobility and eventually resulting in the saturation of drift velocity. This is often referred to as velocity saturation. For electrons, an accurate description of velocity saturation is given by [9]–[11]:

$$v = \frac{\mu \cdot \frac{\partial \psi_s}{\partial x}}{\sqrt{1 + \left(\frac{\mu}{v_{sat}} \cdot \frac{\partial \psi_s}{\partial x}\right)^2}} \quad (2)$$

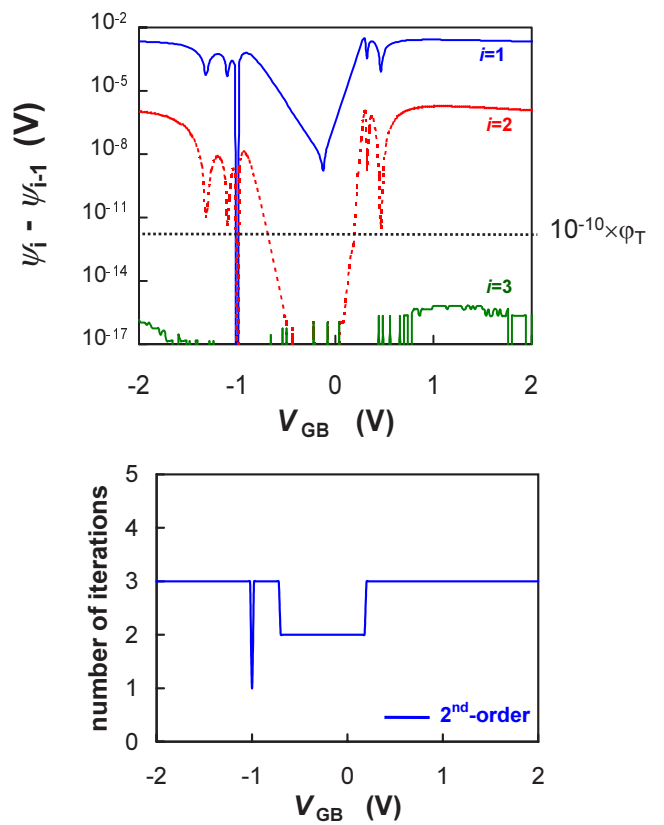


Figure 5: **Top:** Absolute error in surface potential (as a function of gate-bulk voltage) between two successive iterations, where the number of 2nd-order Newton-Raphson iterations is indicated by i . **Bottom:** Number of iterations that is needed to obtain an absolute error in surface potential between two successive iterations smaller than 10^{-10} times the thermal voltage.

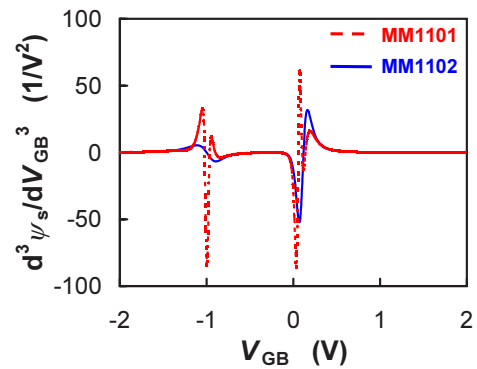


Figure 6: Third-order derivative of the surface potential with respect to the gate-bulk voltage for both level 1101 and level 1102 of MOS Model 11.

where μ is the mobility and v_{sat} is the saturation velocity. This expression can be incorporated in the drain-source channel current I_{DS} by:

$$I_{\text{DS}} = -\frac{\mu \cdot W \cdot Q_{\text{inv}}^*}{\sqrt{1 + \left(\frac{\mu}{v_{\text{sat}}} \cdot \frac{\partial \psi_s}{\partial x}\right)^2}} \cdot \frac{\partial \psi_s}{\partial x} \quad (3)$$

where Q_{inv} is the inversion-layer charge density, and Q_{inv}^* is given by:

$$Q_{\text{inv}}^* = Q_{\text{inv}} - \phi_T \cdot \frac{\partial Q_{\text{inv}}}{\partial \psi_s} \quad (4)$$

The above differential equation (3) for I_{DS} is complicated, and is generally approximated by:

$$I_{\text{DS}} = -\frac{\mu \cdot W}{G_{\text{vsat}} \cdot L} \cdot \int_{\psi_{s0}}^{\psi_{sL}} Q_{\text{inv}}^* \cdot d\psi_s \quad (5)$$

where:

$$G_{\text{vsat}} = \frac{1}{L} \cdot \int_0^L \sqrt{1 + \left(\frac{\mu}{v_{\text{sat}}} \cdot \frac{\partial \psi_s}{\partial x}\right)^2} \cdot dx \quad (6)$$

A first-order approximation of the integral in (6) can be obtained by assuming that the lateral field $-\partial \psi_s / \partial x$ is constant along the channel and equal to $\Delta \psi / L$ [10], [11]. In MM1101, a slightly better approximation of (6) is obtained by assuming that the lateral field $-\partial \psi_s / \partial x$ increases linearly along the channel from 0 at the source to $2 \cdot \Delta \psi / L$ at the drain. In this case, G_{vsat} is given by:

$$G_{\text{vsat}} = \frac{1}{2} \cdot \left[\sqrt{1 + \Gamma^2} + \frac{\ln(\Gamma + \sqrt{1 + \Gamma^2})}{\Gamma} \right] \quad (7)$$

where:

$$\Gamma = 2 \cdot \frac{\mu}{v_{\text{sat}}} \cdot \frac{\Delta \psi}{L} \quad (8)$$

As mentioned before, the above expression for velocity saturation results in an accurate description of the output $I_{\text{D}}-V_{\text{DS}}$ characteristics, but it nevertheless gives a slightly inaccurate description of transconductance g_m in the saturation region, see Figure 7 (top).

In MM1102, velocity saturation is incorporated in a more physical and consequently more accurate way. The differential equation (3) for I_{DS} is rewritten to:

$$I_{\text{DS}} = \sqrt{(\mu \cdot W \cdot Q_{\text{inv}}^*)^2 - \left(\frac{\mu}{v_{\text{sat}}} \cdot I_{\text{DS}}\right)^2} \cdot \frac{\partial \psi_s}{\partial x} \quad (9)$$

Under the correct linearisation of Q_{inv}^* with respect to ψ_s , the above expression can be integrated along the channel from source to drain, resulting in an implicit relation for I_{DS} . Next, the resulting relation is approximated by a third-order Taylor expansion around

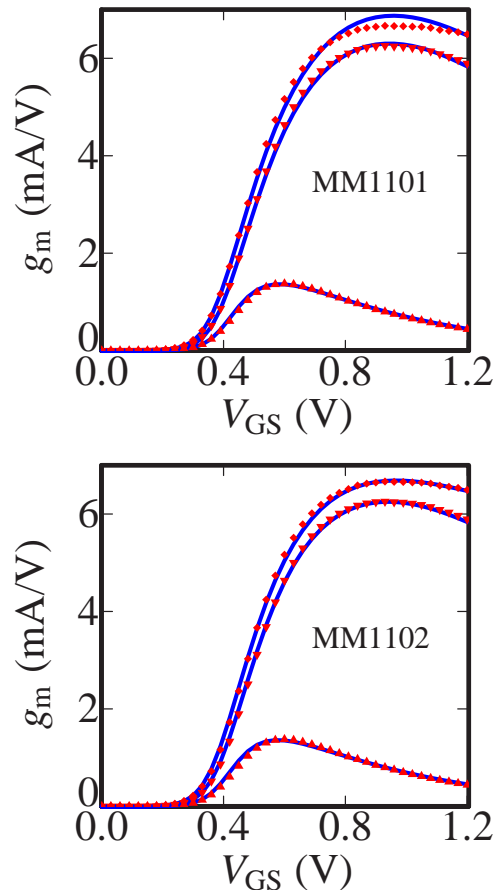


Figure 7: Transconductance of an n-channel MOSFET with $W/L=10\mu\text{m}/0.13\mu\text{m}$ as a function of V_{GS} at $V_{\text{DS}} = 0.05, 0.6, \text{ and } 1.2\text{V}$ and $V_{\text{SB}} = 0\text{V}$. Symbols indicate measurements; lines indicate model calculations with MM1101 (**top**), and MM1102 (**bottom**).

$I_{\text{DS}} = 0$, which again leads to (5) where in this case G_{vsat} is given by:

$$G_{\text{vsat}} = \frac{1}{2} \cdot \left[1 + \sqrt{1 + \frac{\Gamma^2}{2}} \right] \quad (10)$$

The above G_{vsat} -expression is simpler than the MM1101-expression, nevertheless it gives a more accurate description of g_m in the saturation region, see Figure 7 (bottom). As a result, MM1102 gives a more accurate description of distortion than MM1101, see Figure 8.

4 IMPROVED NOISE DESCRIPTION

4.1 Introduction

Accurate compact modeling of noise is a prerequisite for RF CMOS circuit design. At the RF-frequencies used, besides the drain current thermal noise also the

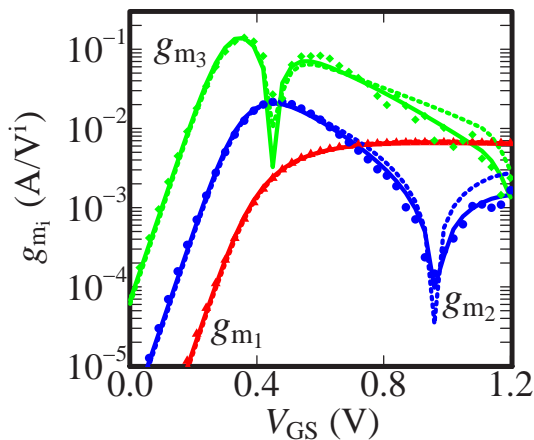


Figure 8: First- (g_{m1}), second- (g_{m2}), and third-order (g_{m3}) derivatives of the drain current with respect to the gate voltage as a function of V_{GS} at $V_{DS} = 1.2\text{V}$ for the device of Figure 7. Symbols indicate measurements; solid lines and dashed lines indicate model calculations with MM1102 and MM1101, respectively.

induced gate noise plays an important role. Over the years, several compact models for induced gate noise have been introduced [12]–[15]. Nevertheless, all of these models are based on the same Van der Ziel model [12], which is only valid in saturation. In addition, the Van der Ziel model is based on the Klaassen-Prins (KP) equation [16], which does not accurately account for velocity saturation [17]. As a result, the above models are inaccurate for short-channel devices, and more accurate modeling for induced gate noise is needed.

4.2 Correct Incorporation of Velocity Saturation in Noise Model

We use an improved KP-approach [18], where fluctuations in the velocity saturation term are also taken into account. Under the appropriate linearisations, the improved approach can be solved in the ψ_s -framework. The above noise model has been implemented in MM1102, where the impact of series resistance and short-channel effects (CLM, DIBL, etc.) have been incorporated as well. To be able to use the compact model for RF-applications, we furthermore extend the model with a gate resistor and a bulk resistance network.

4.3 Experimental results

Noise measurements were performed on $0.18\mu\text{m}$ and $0.12\mu\text{m}$ RF CMOS technologies. Compact model parameters were extracted from DC-measurements, and gate and bulk resistance values were determined from Y -parameter measurements. In Figure 9, noise results are shown for a $L = 0.5\mu\text{m}$ MOSFET. MM1102 based on the improved KP-approach is in excellent agreement with the data without any additional noise parameter

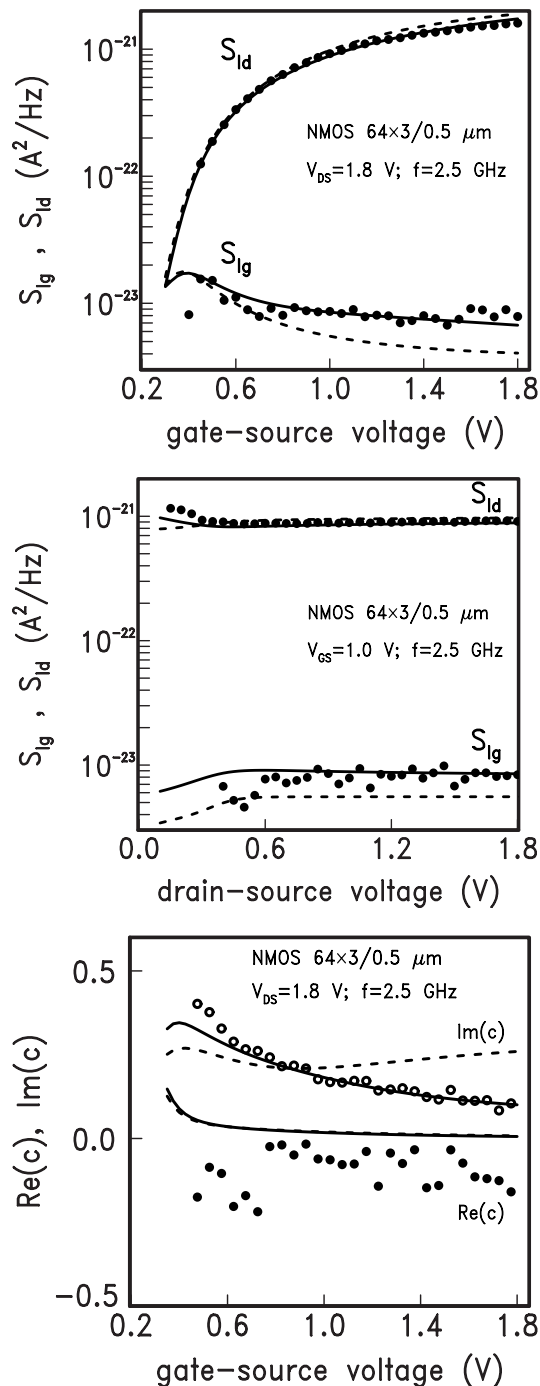


Figure 9: Drain and gate current noise versus gate-source bias (**top**) and versus drain-source bias (**middle**), and correlation coefficient c versus gate-source bias (**bottom**) for an $L = 0.5\mu\text{m}$ n -channel device in $0.18\mu\text{m}$ CMOS technology. Symbols denote measurements, dashed lines denote the Van der Ziel model, and solid lines denote MM1102 based on the improved KP-approach.

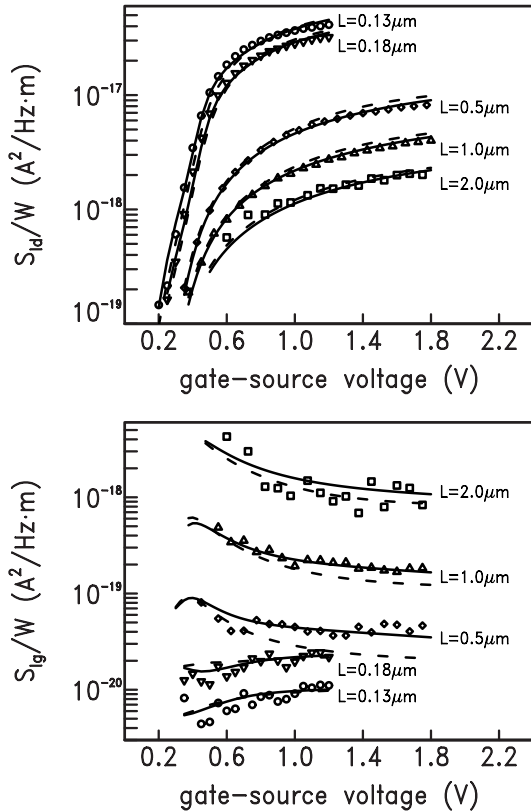


Figure 10: Drain current noise (**top**) and gate current noise (**bottom**) versus gate-source bias for n -channel devices with different channel length L . Symbols denote measurements, dashed lines denote Van der Ziel model, and solid lines denote MM1102 based on the improved KP-approach. ($f = 5\text{GHz}$ and $V_{DS} = 1.0\text{V}$ for $L \leq 0.18\mu\text{m}$, $f = 2.5\text{GHz}$ and $V_{DS} = 1.8\text{V}$ for $L \geq 0.5\mu\text{m}$)

fitting. The Van der Ziel model, on the other hand, leads to a considerable error in the gate noise. The measured real part of c is slightly negative due to non-quasi-static effects, which are not taken into account in the modelling. Noise results for various channel lengths L are shown in Figure 10. MM1102 gives accurate results over all bias conditions and channel lengths. Using the Van der Ziel model leads to an underestimation of gate noise (up to 40%), particularly for intermediate L where velocity saturation is important. For short-channel devices, the differences between the two models are obscured due to the dominant impact of gate resistance (see e.g. [18]).

5 SUMMARY

The newest update of MOS Model 11, level 1102 (MM1102), which is now under test, includes: *i*) an iterative solution of the surface potential; *ii*) an improved

description of the velocity saturation yielding a better modelling of the transconductance in saturation; and *iii*) a better description of noise, especially the induced gate current noise.

The iterative solution results in a more accurate description of surface potential. It has as additional advantage that new physical effects are easily added to the iterative scheme, while for an analytical approximation tedious algebra and often additional approximations for the individual physical effects have to be made. This also implies that: *i*) code maintenance is easier for an iterative solution scheme, and *ii*) the increase in simulation time is very limited. In fact, during test runs with MM1102 on circuits containing several hundreds of transistors an increase in simulation time of only 2 to 3 percent has been observed, while retaining the excellent convergence behaviour of MM1101.

More details and the code of MOS Model 11, level 1102, can be found on our website [19].

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