

Physics-Based, Non-Charge-Sheet Compact Modeling of Double Gate MOSFETs

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ABSTRACT

A physics-based, non-charge-sheet analytic potential model is presented for undoped (or lightly doped) Double Gate (DG) MOSFETs. With only the mobile charge term included, Poisson's equation is rigorously solved and the electrostatic potential is derived analytically. A drain current model is developed afterwards using current continuity equation. It is shown that the model continuously covers all MOSFET operation regions without any fitting parameters. No charge sheet approximation is invoked. Therefore, the model readily captures the volume inversion in the subthreshold region. The derivation is also applied to Surrounding Gate (SGT) MOSFETs, which similarly renders a continuous, closed-form solution of drain current.

Keywords: analytic potential model, compact model, double gate MOSFETs, surrounding gate MOSFETs,

1 INTRODUCTION

Compact models of bulk MOSFETs have evolved from piece-wise models to unified models due to the numerical divergence problem in circuit simulation caused by discontinuous derivatives of MOSFET models. For bulk MOSFETs, one of the reasons that circuit simulation employed piece-wise models is that Pao-Sah's double integral can not be carried out analytically [1]. The charge sheet approximation has to be made to obtain a closed-form, explicit expression of drain current. Fortunately, in DG MOSFETs and SGT MOSFETs, since the silicon film is undoped, depletion charge term does not need to be included in Poisson's equation. This allows exact analytic solutions to Poisson's equation and current continuity equation without the charge-sheet approximation.

2 ANALYTIC POTENTIAL MODEL OF DG MOSFETs [2]

Consider an undoped (or lightly doped), symmetric double-gate MOSFET shown schematically in Fig. 1(a). Poisson's equation along a vertical cut perpendicular to the Si film takes the following form with only the mobile charge (electrons) term:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon_{si}} n_i e^{q(\psi-V)/kT} \quad (1)$$

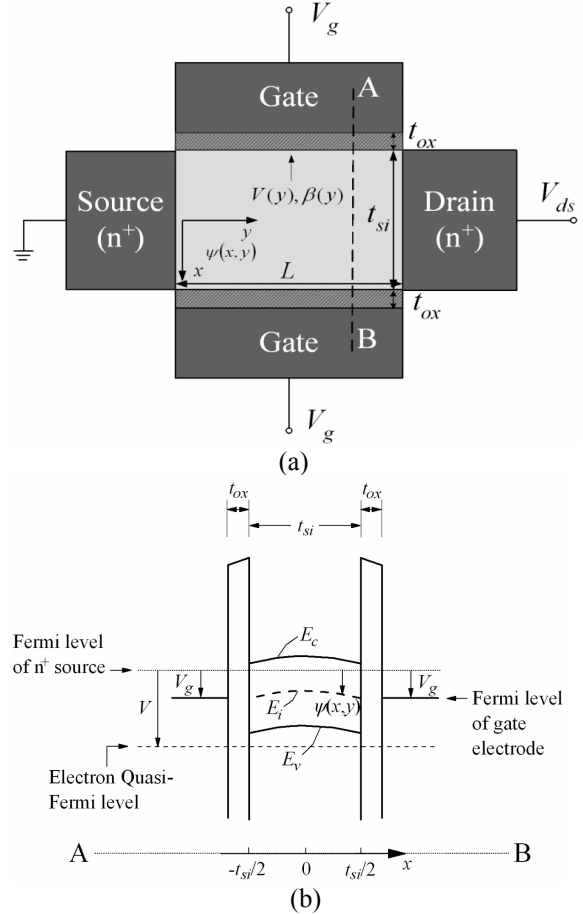


Fig.1. (a) Schematic diagram of a double-gate MOSFET. $V(y)$ is the quasi-Fermi potential at a point in the channel. β is a function of V . (b) Band diagram along a vertical cut (AB) in (a). The potential $\psi(x,y)$ is defined as the intrinsic Si (midgap) level referenced to the Fermi level of the n^+ source as shown (so that $n=n_i$ where $\psi=0$).

where q is the electronic charge, ϵ_{si} is the permittivity of silicon, n_i is the intrinsic carrier density, $\psi(x)$ is the electrostatic potential (reference shown in Fig. 1(b)) and V is the electron quasi-Fermi potential. Here we consider an nMOSFET with $q\psi/kT \gg 1$ so that the hole density is negligible.

Gradual channel approximation assumes the quasi-Fermi potential V stays constant along the x direction (perpendicular to the channel) since the current flows along the y direction (along the channel). Eq. (1) can then be integrated twice to yield the solution [3]

$$\psi(x) = V - \frac{2kT}{q} \ln \left[\frac{t_{si}}{2\beta} \sqrt{\frac{q^2 n_i}{2\epsilon_{si} kT}} \cos \left(\frac{2\beta x}{t_{si}} \right) \right] \quad (2)$$

where β is a function of y (independent of x) to be determined from the boundary condition

$$\epsilon_{ox} \frac{V_g - \Delta\phi - \psi(x = \pm t_{si}/2)}{t_{ox}} = \pm \epsilon_{si} \frac{d\psi}{dx} \Big|_{x=\pm t_{si}/2} \quad (3)$$

Here ϵ_{ox} is the permittivity of oxide, V_g is the voltage applied to both gates, t_{si} and t_{ox} are the silicon and oxide thicknesses, and $\Delta\phi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon. Substituting (2) into (3) leads to

$$\frac{q(V_g - \Delta\phi - V)}{kT} - \ln \left[\frac{2}{t_{si}} \sqrt{\frac{2\epsilon_{si} kT}{q^2 n_i}} \right] = \ln \beta - \ln [\cos \beta] + 2r\beta \tan \beta \quad (4)$$

where $r = \epsilon_{si} t_{ox} / \epsilon_{ox} t_{si}$. By changing the variable in the integral from V to β , current continuity equation can be written

$$I_{ds} = \mu \frac{W}{L} \int_0^{V_{ds}} Q_i(V) dV = \mu \frac{W}{L} \int_{\beta_s}^{\beta_d} Q_i(\beta) \frac{dV}{d\beta} d\beta \quad (5)$$

where β_s, β_d are solutions to Eq. (4) corresponding to $V=0$ and $V=V_{ds}$, respectively. From Gauss's law, $Q_i = 2\epsilon_{si}(d\psi/dx)_{x=t_{si}/2}$, which is simply $2\epsilon_{si}(2kT/q)(2\beta/t_{si})\tan\beta$ using Eq. (2). $dV/d\beta$ can also be expressed as a function of β by differentiating Eq. (4). Substituting these factors in Eq. (5) allows the integration to be carried out analytically:

$$I_{ds} = \mu \frac{W}{L} \frac{4\epsilon_{si}}{t_{si}} \left(\frac{2kT}{q} \right)^2 \times \left[\beta \tan \beta - \frac{\beta^2}{2} + r\beta^2 \tan^2 \beta \right] \Big|_{\beta_d}^{\beta_s} \quad (6)$$

With β as an intermediary parameter, the drain current of all operation regions is included in this analytic expression. Piece-wise, explicit expressions of drain current can be obtained from Eq. (6) by making approximations of Eq. (4) and (6) in different regions. For example, in the linear region above threshold, the right hand side of Eq. (4) and (6) is dominated by their last terms. Therefore,

$$I_{ds} = 2\mu C_{ox} \frac{W}{L} (V_g - V_t - V_{ds}/2) V_{ds} \quad (7)$$

where $V_t = V_0 + \delta$ with

$$V_0 = \Delta\phi + 2kT/q \ln \left[2\sqrt{2\epsilon_{si} kT / q^2 n_i} / t_{si} \right] \quad (8)$$

$$\delta = 2kT/q \ln \left[q(V_g - V_0) / 4rkT \right] \quad (9)$$

Here V_t is the threshold voltage of DG MOSFETs and is independent of t_{si} [2].

Similarly, the current for the saturation region and the subthreshold region can be approximated as follows, respectively.

$$I_{ds} = \mu C_{ox} \frac{W}{L} \left[(V_g - V_t)^2 - \frac{8rk^2 T^2}{q^2} e^{q(V_g - V_0 - V_{ds})/kT} \right] \quad (10)$$

$$I_{ds} = \mu \frac{W}{L} kT n_i t_{si} e^{q(V_g - \Delta\phi)/kT} (1 - e^{-qV_{ds}/kT}) \quad (11)$$

Note that the subthreshold current is proportional to the silicon thickness t_{si} , but independent of t_{ox} —a manifestation of “volume inversion” that cannot be reproduced by standard charge-sheet-based I-V models. In contrast, the above threshold currents, Eq. (7) and (10), are proportional to C_{ox} , but independent of silicon film thickness. These observations show that the essential physics are preserved in this continuous, analytic model.

Fig. 2 illustrates the current with respect to gate voltage computed from the model. A constant mobility of 300 cm/V.S is assumed here. As expected, two currents with different t_{si} only differ in the subthreshold region. After the DG MOSFET turns on, the drain current is independent of the silicon film thickness.

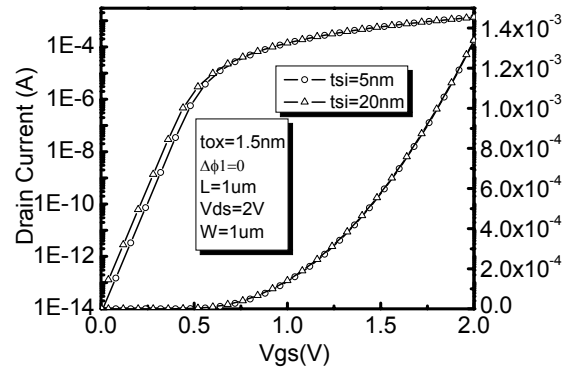


Fig. 2. I_{ds} - V_{gs} characteristics obtained from the analytic model for two different values of t_{si} . The same currents are plotted on both logarithmic (left) and linear (right) scales.

3 ANALYTIC POTENTIAL MODEL OF SGT MOSFETS

SGT MOSFETs have better scalability than DG MOSFETs due to the tighter control of electrostatic potential by the all-around gate [4]. The drain current model of SGT MOSFETs is developed by Jiménez *et al.* [5] following the publication of DG MOSFET model by Taur *et al.* [2]. The derivation is analogous to DG MOSFETs and is summarized as follows.

Fig.3 illustrates the cross sections of the SGT MOSFET. In cylindrical coordinates, Poisson's equation takes the following form for undoped MOSFETs

$$\frac{d^2\psi}{dr^2} + \frac{1}{r} \frac{d\psi}{dr} = \frac{q}{\epsilon_{si}} n_i e^{\frac{q(\psi-V)}{kT}} \quad (12)$$

With the same gradual channel approximation, integrating (12) twice gives the electrostatic potential along the radial direction:

$$\psi(r) = V + \frac{kT}{q} \ln \left[\frac{-8kT\epsilon_{si}B}{q^2 n_i (1 + Br^2)^2} \right] \quad (13)$$

where B is a constant (of r) to be determined by the boundary condition

$$C_{ox}(V_{gs} - \Delta\phi - \psi_s) = \epsilon_{si} \left. \frac{d\psi}{dr} \right|_{r=R} \quad (14)$$

Note that here the oxide capacitance per area is defined differently

$$C_{ox} = \frac{\epsilon_{ox}}{R \ln(1 + t_{ox}/R)} \quad (15)$$

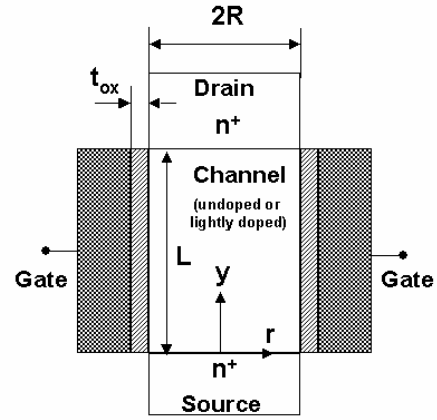
Thus the total capacitance is $2\pi R L C_{ox}$.

Substituting (13) into (14) leads to

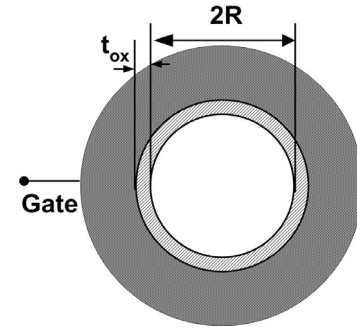
$$\frac{q(V_{gs} - \Delta\phi - V)}{kT} - \ln \left(\frac{8kT\epsilon_{si}}{q^2 n_i R^2} \right) = \ln(1 - \beta) - \ln \beta^2 + \eta \left(\frac{1 - \beta}{\beta} \right) \quad (16)$$

where $\beta = 1 + BR^2$ is a constant (of r) to be determined by (16), and $\eta = 4\epsilon_{si}/C_{ox}R$ is a structural parameter.

Following the same procedure as DG MOSFETs, one could apply current continuity equation (5) and substitute Q_i and $dV/d\beta$ of SGT MOSFETs into (5) to derive the drain current



(a)



(b)

Fig. 3 The cross sections of the SGT-MOSFET. (a): the cross section along the channel direction. (b): the cross section perpendicular to the channel direction

$$I_{ds} = \mu \frac{4\pi\epsilon_{si}}{L} \left(\frac{2kT}{q} \right)^2 \left[\frac{\eta}{4\beta^2} + \frac{1 - \eta/2}{\beta} + \frac{1}{2} \ln \beta \right] \Bigg|_{\beta_d}^{\beta_s} \quad (17)$$

where β_s, β_d are solutions to Eq. (16) corresponding to $V=0$ and $V=V_{ds}$, respectively.

Approximations can be made to obtain explicit expressions with gate and drain voltages for different biasing regions.

1: Subthreshold region

$$I_{ds} = \mu \frac{\pi R^2}{L} n_i k T e^{\frac{q(V_{gs} - \Delta\phi)}{kT}} \left(1 - e^{-\frac{qV_{ds}}{kT}} \right) \quad (18)$$

Volume inversion occurs in the subthreshold region as it can be seen that the drain current is proportional to the area of the cross section, πR^2 .

2: Linear region above threshold:

$$I_{ds} = 2\mu C_{ox} \frac{\pi R}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}. \quad (19)$$

where V_t is the threshold voltage of SGT MOSFETs

$$V_t = \Delta\phi + \frac{kT}{q} \ln \left(\frac{8kT\epsilon_{si}}{q^2 n_i} \right) - \frac{2kT}{q} \ln \left(R \left(1 + \frac{t_{ox}}{R} \right)^{\frac{2\epsilon_{si}}{\epsilon_{ox}}} \right). \quad (20)$$

Note that V_t of SGT MOSFETs is a function of R , which is contrary to DG MOSFETs whose threshold voltage is independent of t_{si} .

3: Saturation region:

$$I_{ds} = \mu C_{ox} \frac{\pi R}{L} \left\{ \left(V_{gs} - V_t \right)^2 - \left(\frac{kT}{q} \right)^2 \left[\frac{\eta^2}{\left(1 - e^{-\frac{q(V_{gs}-V_0-V_{ds})}{kT}} \right)^2} + \frac{4\eta(1-\eta/2)}{\left(1 - e^{-\frac{q(V_{gs}-V_0-V_{ds})}{kT}} \right)} \right] \right\}. \quad (21)$$

Fig.4 shows the drain current as a function of gate voltage with two different values of R . The curves show that both the on-current and the off-current are dependent on R . It is expected from the explicit expressions that the subthreshold current has much stronger dependence on R than the on-current. As seen from the figure, the subthreshold current ratio between $R=20\text{nm}$ and 5nm is around 16 (square dependence on R), whereas the on-current ratio between the two curves is around 4 (approximately linear dependence on R).

Although the derivation of SGT MOSFETs renders a similar drain current expression as DG MOSFETs, some of the different characteristics are noteworthy. For SGT MOSFETs, both the on-current and the off-current are dependent on the radius R . The on/off current ratio is approximately proportional to $1/R$. Thus thin body SGT MOSFETs with small radius will be more favourable for a high on/off current ratio. For DG MOSFETs, the on/off current ratio is proportional to $1/t_{si}$. Thus one should keep R smaller than t_{si} in order to obtain a higher on/off current ratio. While smaller radius is beneficial, the thin body SGT MOSFET delivers rather limited drive current due to its short perimeter compared with the width of DG MOSFETs. One feasible solution to enhance the current drivability is to use multi-pillar SGT MOSFETs [6]. With each pillar's radius R smaller than t_{si} and with a sufficiently large number of pillars, high on-off current ratio as well as high drive current can be achieved for SGT MOSFETs. Further,

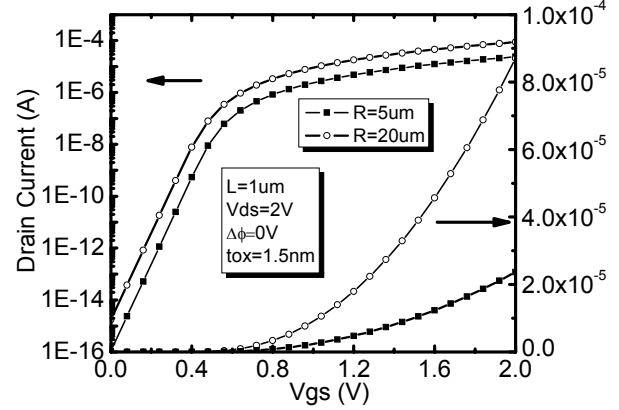


Fig. 4. $I_{ds}-V_{gs}$ characteristics obtained from the analytic model for two different values of R . The same currents are plotted on both logarithmic (left) and linear (right) scales.

small radius is also desirable for better short channel effect. S.-H. Oh *et al.* proposed an analytic description of the short channel effect for SGT and DG MOSFETs [4]. It is estimated that when $R=0.76t_{si}+3.3t_{ox}$, SGT and DG MOSFETs have the same scale length. Therefore, for SGT MOSFETs to gain superiority over DG MOSFETs, R should be smaller than t_{si} considering both the short channel effect and the on/off current ratio.

4 CONCLUSIONS

In conclusion, an analytic potential model of drain current for DG MOSFETs as well as SGT MOSFETs is developed. The model is predictive since it physically preserves the attributes of DG MOSFETs. Moreover, the model is suitable for circuit simulation as it is continuously valid in all biasing regions. These characteristics enable the model to be a kernel for DG MOSFET models. The intrinsic charges and capacitances can be modeled based on the drain current expression. Furthermore, additional physical models for short channel effect, quantum effect, etc. should also be developed in order to build a complete DG MOSFET model.

REFERENCES

- [1] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, New York, 1998.
- [2] Y. Taur, X. Liang, W. Wang and H. Lu, "A continuous, analytic drain-current model for DG-MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107-109, Feb. 2004.
- [3] Y. Taur, "An Analytical Solution to a Double-Gate MOSFET with Undoped Body," *IEEE Electron Device Lett.*, Vol. 21, No. 5, pp. 245-247, May 2000.

- [4] S. H. Oh, D. Monroe and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445-447, Sep. 2000.
- [5] D. Jiménez, B. Iñíguez, J. Suñé, L. F. Marsal, J. Pallarès, J. Roig and D. Flores, "Continuous analytic current-voltage model for surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 251, no. 8, pp. 571-573, Aug. 2004.
- [6] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi and F. Masuoka, "Multi-pillar surrounding gate transistor (M-SGT) for compact and high-speed circuits," *IEEE Trans. Electron Devices*, Vol. 21 ,no.9 , pp. 579 – 583 Mar. 1991