A Study of Figures of Merit for High Frequency Behavior of MOSFETs in RF IC Applications

Yuhua Cheng

Siliconlinx, Inc., Irvine, California, USA, yuhua.cheng@siliconlinx.com

ABSTRACT

This paper is to review important device parameters as the figures of merit (FOM) to understand the device characteristics for analog/RF applications. These FOM should be characterized and evaluated in technology development and model generation for analog/RF technologies. This paper has tried to show these FOM with both measured data and model simulation to help both technology developers and modelers in developing high performance advanced processes and generating high quality accurate models. Device models generated with validations based on these FOM will greatly help circuit designers in designing robust and high performance analog/RF IC circuits.

Keywords: MOSFET figures of merit; MOSFET modeling; MOS Transistor, CMOS circuit design, RF modeling

1 INTRODUCTION

Recent speed improvements of digital sub-micron bulk CMOS transistors have made it feasible to implement RF circuits operating at Giga Hz range. Currently, RF designers are exploring CMOS technology as a lower cost solution for various RF applications. In digital circuit applications, several device parameters such as I_{dsat}, I_{off} and gate delay have become standard figures of merit (FOM) to evaluate MOSFET performance between circuit designers and device technology developers. However, it has not been the case for analog/RF applications. Even though many device parameters have been used by designers in optimizing circuit performance, only some of them are used by process developers as targets for analog/RF process development. A complete set of device parameters have not been put together as FOM to evaluate device behavior between designers and process developers, especially for modelers to use in generating and qualifying device models for analog/RF applications. One reason is that device technology developers have not paid enough attentions to optimize CMOS technologies by using a full set of FOM for different analog/RF applications. It is a challenging effort and will take some time for CMOS technology developers to get familiar with these FOM and use them in guiding the process development. Currently only some efforts have been made in defining various tests to qualify device models, starting from DC ones and now getting into high frequency cases. However, even these tests are not all used by the model developers and modelers who perform only a subset of these tests in generating device models for designers. Without careful examinations based on certain FOM, sometimes these models could be wrong in predicting device behavior for specific RF applications. Therefore, it is very critical for model developers to qualify the models with a set of FOM (as complete as possible) for analog/RF applications in order to create accurate and physical models.

This paper will review device parameters in MOSFETs for analog/RF applications. This work addresses these FOM with both measured data and model simulation to initiate the efforts in using these FOM for technology development and model validations. Model validation and qualifications based on these FOM should be performed when generating device models for analog/RF circuit applications.

2 REVIEW OF IMPORTANT DEVICE PARAMETERS AND FOM DISCUSSION

As FOM, I_{dsat}, I_{off} and gate delay have been widely used for digital applications. Usually, I_{dsat} is defined as the drain current I_D when gate-source voltage V_{GS}=V_{DD} and drain-source voltage V_{DS}=V_{DD}, and I_{off} is defined as the I_D when V_{GS}=0V and V_{DS}=V_{DD}, as shown in Fig. 1. A parameter called threshold voltage, V_{TH}, is also introduced. Many definitions for V_{TH} have been invented, but only two of them are commonly adopted. One is the maximum trans-conductance (G_m) method, which takes the V_{GS} extrapolated linearly from I_D-V_{GS} curve at the point of maximum G_m, and another one is the constant current method, which takes the V_{GS} at a specific drain current [1]. This specific current has been taken as somewhat arbitrary, however, it can be considered as I_S, a function of device geometry, mobility and temperature as discussed in [2]. V_{TH} defined based on the constant current I_S is easier to measure than the one by the maximum G_m method, especially for the devices with very short channel lengths. Based on I_S, one parameter Inversion Coefficient (IC) has been proposed as a measure of MOS inversion level to describe the MOSFET operation for analog applications [2]. IC is a ratio of I_D/I_S. In weak inversion, IC<<1, and in strong inversion, IC>>1 while in moderate inversion IC≅1.

G_m is one of the most important parameters in analog/RF design and is also the one that process developers would look at in developing an analog process. As shown in Fig. 2, G_m at given current is higher in the device in newer technology nodes. A parameter G_m/I_D has been proposed to evaluate the device performance, the transconductance efficiency, for analog design [2]. This has become a widely adopted FOM of MOSFET. This has also been proposed as a standard test used for model validation to check if the model has met the requirements in analog design. As shown in Fig. 2, G_m/I_D maximizes in weak inversion region and reduces rapidly in moderate inversion region while approaching its minimum at strong inversion. The G_m/I_D ratio has been considered a universal characteristic of all transistors formed by the same process. It could indicate how power efficient of a MOSFET in moderate inversion (subthreshold) region. Based on this factor, analog circuits could be optimized while other factors such as I_D and size parameters are also considered.

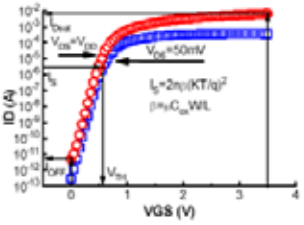

Fig. 1. Illustrations of I_{dsat}, I_{off}, I_S, and V_{TH}.

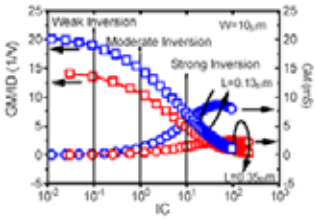

Fig. 2. G_m/I_D illustration.

C_{gg}/I_D is one parameter but it is not commonly referred, where C_{gg} is the total gate capacitance. It can be considered as the delay per voltage as a FOM to evaluate the device speed. As shown in Fig. 3 with the data from two different (0.35 and 0.18µm) technology node, this parameter is not sensitive to the bias conditions at given I_D. The smaller the C_{gg}/I_D, the better (faster) the device.

Current gain, h_{21}, is used often in BJT devices but less in MOSFETs. It can be defined as:

$$h21 = \frac{y21}{y11} \tag{1}$$

Fig. 4 illustrates the characteristics of h_{21} vs. I_D. Actually, people prefer to use real(y_{21}) in estimating the current gain of the device for that it is linked to the DC G_m of the device as shown in Fig. 5.

Another parameter has been correlated closely with current gain is f_T. f_T is often called transit frequency and has been widely used to demonstrate device behavior at high frequency (HF) and validate models. f_T is defined as the frequency at which the current gain, h_{21}, of the device equals to 1. According to this definition, the following simple expression can be derived for f_T [3],

$$fT = \frac{Gm}{2 \cdot \pi \cdot Cgg} \tag{2}$$

f_T at given bias conditions can be obtained from the measured data of the gain h_{21} vs. frequency by

$$fT = -imag(h21) \cdot fo \tag{3}$$

where f_o is a constant frequency selected in the frequency range with the slope of h_{21} of –20dB/dec (usually 1~3 GHz depending on the technology nodes).

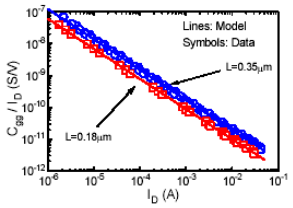

Fig. 3 Measured and Modeled C_{gg}/I_D characteristics.

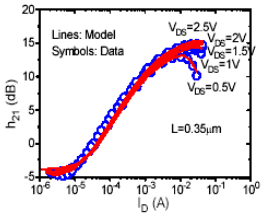

Fig. 4 Curves of h_{21} vs. I_D.

f_T is also a measure of the speed of the device. The characteristics of f_T vs. I_D are shown in Fig. 6 for three different (0.35µm, 0.18µm and 0.13µm) technology nodes. This FOM has been widely used to demonstrate the device performance and model accuracy by technology developers and modelers. However, in today's very advanced technologies such as 0.13um and 90nm nodes, f_T alone may not be a good parameter to understand the HF behavior of a MOSFET for RF circuit applications. In another word, one should look at not only the f_T behavior but also some other device parameters, such as power gain and f_{max} to be discussed next, to fully understand and evaluate the device performance for RF applications.

The maximum power gain, $G_{T,max}$ can be derived as [4]

$$GT,\max = \left|\frac{S21}{S12}\right|\left(K - \sqrt{K^2 - 1}\right) \tag{4}$$

$$K = \frac{1 - |S11|^2 - |S22|^2 + |S11S22 - S12S21|^2}{2|S12S21|} \tag{5}$$

Where K is the stability factor. The maximum stable power gain is defined as the $G_{T,max}$ when K=1, that is

$$GST,\max = \left|\frac{S21}{S12}\right| \tag{6}$$

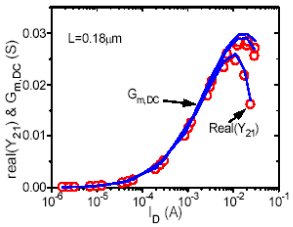

Fig. 5 $G_{m,DC}$ and Real(Y_{21}).

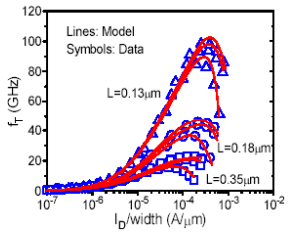

Fig. 6 f_T vs. I_D/W.

For a single MOS transistor, the maximum stable power gain is a FOM together with f_T to describe the HF performance of the device. Actually for real RF circuit design, $Gs_{T,max}$, the maximum power gain delivered by the device, may be more useful than f_T to guide the circuit design. Fig. 7 illustrates $Gs_{T,max}$ of devices from several different (0.35µm, 0.18µm and 0.13µm) technology nodes.

Different from the f_T behavior given in Fig. 6, the devices in newer technology nodes show somewhat higher power gain at given current density but not very significantly while devices with longer lengths in the same technology show obvious reduction of power gain (not shown in the figure). In addition to f_T, power gain should be a FOM for modelers to validate the models, even though, usually, this parameter could be modeled well if the DC and AC model parameters are extracted correctly.

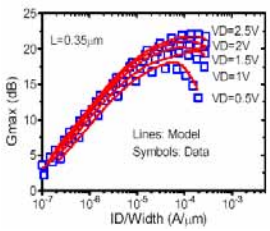

Fig. 7 Power gain vs. I_D.

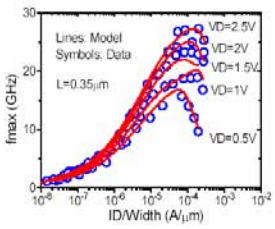

Fig. 8 f_{max} vs. I_D.

Associated with $Gs_{T,max}$, f_{max} is an alternative FOM to describe the HF performance of the device. f_{max} is called the maximum frequency of oscillation, and is the frequency at which the maximum power gain equals to 1. f_{max} contains the impacts from parasitics such as gate and substrate resistance and is a better FOM than f_T for HF behavior of MOSFETs even though it is a little difficult to measure. Fig. 8 illustrates the characteristics of f_{max} vs. I_D for a device with channel length of 0.35μm.

Furthermore, some device parameters can be derived from y parameters in a more meaningful format for circuit designers, such as input resistance and capacitance, R_{in} and C_{in}; output resistance and capacitance R_{out} and C_{out}; feedback resistance and capacitance R_{fb} and C_{fb}.

The input resistance and capacitance is defined as

$$R_{in} = real\left(\frac{1}{y11}\right); \text{ and } C_{in} = \frac{-1}{\omega \cdot imag\left(1/y11\right)} \quad (7)$$

$$R_{out} = real\left(\frac{1}{y22}\right); \text{ and } C_{out} = \frac{imag(y22)}{\omega} \quad (8)$$

$$R_{fb} = real\left(\frac{-1}{y12}\right); \text{ and } C_{fb} = \frac{1}{\omega \cdot imag\left(1/y12\right)} \quad (9)$$

It should be noted that these parameters are sensitive to the bias dependence of gate resistance and capacitance and could provide the information circuit designers would like to have. Thus they are useful FOM, especially for model validation. However, Specific care in model parameter extraction is needed for a model to predict correctly these parameters. Fig. 9 and Fig. 10 illustrate measured and modeled curves for these parameters.

Flicker noise is another device parameter in analog and RF applications. People often extract a model parameter called K_F to compare flicker noise performance of different technologies based on the measured data as shown in Fig. 11 [5]. However, it is more straightforward to use the corner frequency F_{corner} as a FOM to evaluate the flicker noise behavior. F_{corner} is the frequency above which the noise amplitude is approximately equivalent to the thermal noises as shown in Fig. 12. Note that F_{corner} for the voltage noise may be different from the F_{corner} for the current noise. F_{corner} is a function of the temperature, bias, and device geometry as well as the fabrication process. Under "typical" operating conditions, the F_{corner} is with values of 100 kHz to 100 MHz, depending on technology and device geometry.

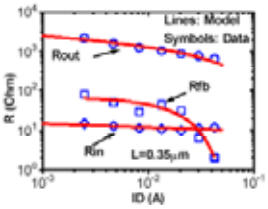

Fig. 9 R_{in}, R_{out}, R_{fb} vs. I_D.

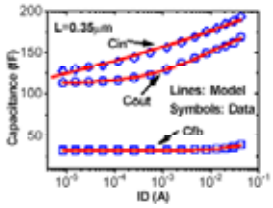

Fig. 10 C_{in}, C_{out}, C_{fb} vs. I_D.

The flicker noise spectral density can be given by the following simplified expression:

$$S_{noise} = \frac{KF \cdot ID \cdot \Delta f}{L^2 \cdot Cox \cdot f} \quad (10)$$

The thermal noise can be expressed approximately by

$$S_{noise} = 4 \cdot k \cdot T \cdot \gamma \cdot Gm \cdot \Delta f \quad (11)$$

Thus based on (1) and (2), and the definition of F_{corner},

$$F_{corner} = \frac{KF}{4 \cdot k \cdot T \cdot \gamma \cdot Cox \cdot L^2 \cdot Gm / ID} \quad (12)$$

It is difficult to measure F_{corner} directly due to the equipment limitation, but based on (12) we could estimate it with the extracted K_F at a fixed G_m/I_D value as a FOM.

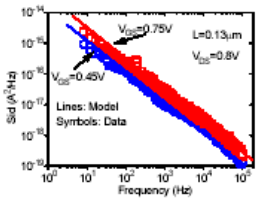

Fig. 11 Measured and Modeled Flicker noise.

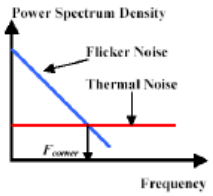

Fig. 12 F_{corner} definition.

In addition to the FOM for low frequency noise, the FOM for HF noise are also required. HF noise is usually characterized by parameters such as the minimum noise figure, the input referred noise resistance and the optimum source admittance [5].

The noise factor is a FOM for a performance of a device or a circuit with respect to noise. The standard definition of the noise factor of a two-port network is the ratio of the available output noise power per unit bandwidth to the portion of that noise caused by the actual source connected to the input terminals of the device. The noise figure of a two-port network is given by [5]

$$NF = NF\min + \frac{4 \cdot rn \cdot |\Gamma s - \Gamma opt|^2}{(1 - |\Gamma s|^2) \cdot |1 + \Gamma opt|^2} \quad (13)$$

where Γ_s and Γ_{opt} are the reflection coefficients, the ratio of the incident to the reflected wave along a transmission line. In the HF noise measurements, the source reflection coefficient is varied until a minimum noise figure is reached. The value of NF_{min}, which occurs when $\Gamma_s = \Gamma_{opt}$, is read from the noise figure meter, and the source reflection coefficient that produces NF_{min} is determined by a network analyzer. The noise resistance r_n is measured by reading the noise figure when Γ_s =0.

N_{Fmin} is a function of the biases (operating current) and frequency. Each N_{Fmin} is associated with one value of $\Gamma_{opt.}$ Fig. 13 (a) shows a typical characteristics of N_{Fmin} vs. frequency for a MOSFET of 0.18μm length. Fig. 13 (b) gives the plot of N_{Fmin} vs bias current.

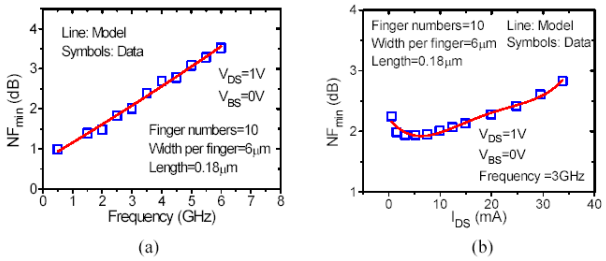

Fig. 13 Measured and fitted (a) N_{Fmin} vs. frequency; (b) N_{Fmin} vs. I_{DS}.

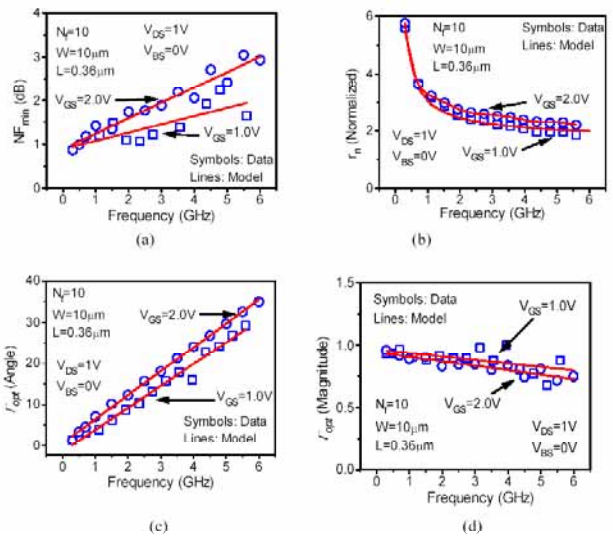

Fig. 14 Comparisons of measured data and simulations at different bias conditions and frequency for (a) NF_{min} (b) the magnitude of the optimized source reflection coefficient Γ_{opt}; (c) the phase of the optimized source reflection coefficient Γ_{opt}; (d) the noise resistance normalized to 50Ω, r_n.

Fig. 14 further demonstrates the measured and simulated results for these FOM parameters used for HF noise characterization. A translation from noise power spectral density, which is commonly used in the noise model development and circuit simulator implementation, to these four parameters can be done with the developed algorithm. Some discussion has been given to understand their correlations between the noise power spectral density and these four noise parameters in describing the HF noise characteristics of the device [6,7]. Nevertheless, these parameters have become commonly used FOM in device characterization and model validation for HF noise behavior of the device. It should be noted that specific care is needed in model parameter extraction for a model to predict the HF noise behavior correctly over the bias and frequency [8].

Recently, designers have started exploring RFCMOS for PA applications. A lot of factors related to electrical, thermal, reliability, and cost etc., should be taken into account to select devices in PA design, however, the most important FOM should be the power efficiency, the linearity and the robustness.

Efficiency of a PA is defined as

$$\eta = \frac{P_{out}}{P_{dc}} \tag{14}$$

where P_{out} is the output RF power and P_{dc} is the supply power. It is a measure of how efficiently the supply power is translated to output power. A 100% η implies that the entire supply power is delivered to the load. However, this is practically impossible to achieve. The best way to improve the efficiency is to use circuit techniques such that both voltage and current waveforms do not exist simultaneously. Switching amplifiers use this approach to achieve efficiencies up to 80%. However, as a trade-off, linearity, which is another FOM to be discussed, needs to be compromised for better efficiency.

Actually, an more often-used FOM when comparing the performance of PAs with different input power levels is the power added efficiency (PAE). PAE is defined as

$$PAE = \frac{P_{out} - P_{\text{int}}}{P_{dc}} \tag{15}$$

where P_{in} is the input power for the power amplifier. It should be noted that PAE could significantly differ from η when the power gain is lower than 10 dB, which can often be the case with power amplifiers.

Determining how active devices behave at different power levels is an important consideration when designing RF circuits. Many RF amplifiers are designed to operate in the weakly nonlinear region, where PAE peaks. Large-signal measurements provide output power, gain, and efficiency information at a given input power level. Simulations of PAE based on a benchmark circuit would be useful in comparing the device performance of MOSFETs for PA applications. Fig. 15 shows the results of P_{in}, P_{out}, gain and PAE.

Linearity is another important metric of a PA. It is desired that the amplifier operate with high linearity i.e., the output power is always linear with input power. However, a device eventually saturates after a certain input power as shown in Fig. 16, and this introduces harmonics in the output power spectrum. Linearity in power

amplifiers is of serious concern because they can be often made to operate in the non-linear region to deliver a large output power. Gate capacitance has been considered as a factor in determining the device linearity in an amplifier. C_{gs} varies substantially as the device transits from an "off" (below threshold) to an "on" (above threshold) state, which leads to substantial distortion at the gate, and can subsequently limit overall amplifier linearity. 1-dB compression and third order intercept points are typically used to measure linearity.

Ss shown in Fig. 16, 1-dB compression is the input power at which the linear gain of the amplifier has compressed by 1 dB. The output referred 1-dB compression point (in dB) would then be given by the sum of the input referred 1-dB point (in dB) and the gain of the amplifier (in dB). This metric is an often-used measure of the linear power handling capability of the PA.

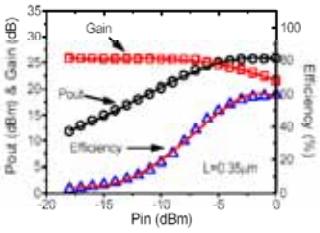

Fig. 15 Illustrations of P_{in}, P_{out}, gain and PAE.

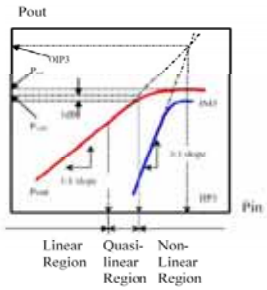

Fig. 16 P_{out} vs. P_{in} Behavior.

Third-order intercept point is a useful metric when comparing RF blocks with different specifications, as it is independent of the input power levels. In the case of two interferers very close to the desired frequency, a non-linear output from the PA will generate inter-modulation products. The most important one of the products is the third order product since it is right in the frequency band of interest. The amplitude of this IM3 product term increases in the order of cube of the fundamental amplitude and can be as significant as the fundamental tone after a certain input power. It has been known that MOS devices deliver lower gain than the bipolar and III-V counterparts. To accommodate this small transconductance, the input signal amplitude has to be increased. Increasing the input signal amplitude can dramatically degrade the PA linearity because the third-order nonlinearity of the device current is directly proportional to the cube of the input voltage amplitude. Thus, higher nonlinearity will be expected for MOS devices even though a higher "low frequency limit" behavior were observed [9].

Fig. 16 shows the important definitions of electrical parameters for large signal modeling and designs. For PA design, another important factor is the robustness consideration due to that the device has to tolerate very high voltage swing during the circuit operation. One parameter to evaluate this is Baliga Figure of Merit [10]:

$$Eb = \left(\frac{4 \cdot V_{bk}^2}{\varepsilon \cdot \mu \cdot R_{on}} \right)^{1/3} \qquad (16)$$

where ε is the relative permittivity of the semiconductor, V_{bk} is the breakdown voltage, E_b is the critical electrical field, R_{on} is the on-state resistance, and μ is the mobility.
It is obvious by the above equation that designers would like to have an as high as possible E_b. It is a FOM widely used in III-V devices. We mention it here to emphasize the importance of MOSFETs' breakdown voltage parameter, which is critical in devices for applications such as PA and now also power management IC.

A good RF model should well predict the large signal behavior of the device over the frequency and biases. Fig. 17 gives the measured and modeled results of P_{out} vs. P_{in} at various input power level. Fig. 18 shows the measured data and model simulation for the characteristics of P_{out} vs I_{DS}. A model with carefully extracted parameters at DC and AC small signal could well predict the large signal behavior of the device, without any additional parameter extraction efforts with the large signal data [9].

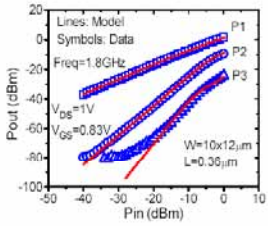

Fig. 17 P_{out} vs. P_{in}

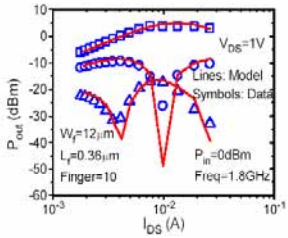

Fig. 18 P_{out} vs I_{DS}.

As another newer trend, CMOS is becoming increasingly interesting for RF switch applications. In many RF applications it is desirable to switch an analog signal on and off without making any impact on the signal. Particularly this is relevant in the front-end of a multi-band radio transceiver where the received and transmitted signals have to be switched between different antennas, filters, amplifiers and mixers. Integrated radio circuits have been using GaAs FET transistors due to their good performance at high frequencies. However, as the size shrinking and speed increasing of MOSFET transistors, there is a great advantage to use the same CMOS process for the whole system, including both analog and digital.

For a device to be used for switch applications, low insertion loss in the on-state and high isolation in the off state as well as high linearity are desirable. Thus, insertion loss, isolation and linearity are discussed as three FOMs to evaluate device performance and validate a MOSFET model targeted for RF switch applications.

Fig. 19 is a schematic for a simple RF switch based on a. single MOSFET. The control and bias voltages will let the transistor operate in its most linear region. So the linearity of the device vs. biases needs to be checked carefully. If the signal power is very high, a significant voltage drop over the transistor exists and the device will

become non-linear. However, at very low signal powers the on resistance, an indication of the loss in on-mode of the switch, of the device is too high. So, the device for use in RF switch circuits should ensure a reasonably good linearity and low on-resistance at a wide bias regime.

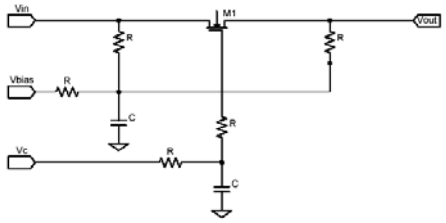

Fig. 19 schematic of a simple single transistor switch.

Loss is naturally an important parameter to be evaluated for a switch. Too high loss in on-mode will make the signal weak and too low loss in off-mode (isolation) will result in signal leakage. High loss in off-mode is especially important for switches separating the transmitter and the receiver while low loss in on-mode is important for switches before the LNA in the receiver.

At high frequency measurements, the loss of a device is usually defined as the power loss resulting from the insertion of the device in a transmission line and is simply called insertion loss (IL). From this definition, the insertion loss of the switch element is directly related S_{21}, which is also related to the on-state resistance of the series switch element as follows,

$$IL(dB) = 10 \cdot \log(P_{in}/P_{out}) = -20 \cdot \log|s21| \quad (17)$$

Also, the isolation can be measured by

$$Isolation\,(dB) = 10 \cdot \log(P_{out}/P_{source}) \quad (18)$$

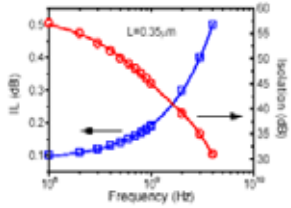

Fig. 20 Insertion loss and isolation vs. frequency

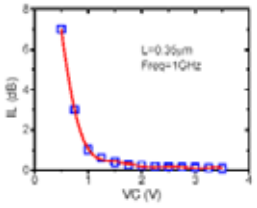

Fig. 21 Insertion loss vs. Vc.

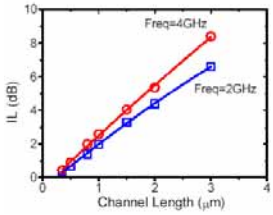

Fig. 22 Insertion loss vs. device channel length *L*.

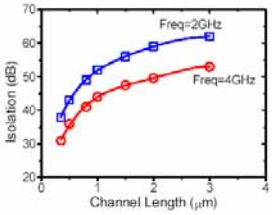

Fig. 23 Isolation vs. *L*.

Fig. 20 illustrates an example of the results of insertion loss and isolation over frequency. Fig. 21 shows an example of the results of insertion loss vs. the control voltage. Furthermore, Fig. 22 and Fig. 23 give the results of the insertion loss and isolation for devices with several different channel lengths. It is a challenging effort to use the conventional CMOS devices for RF switch applications, however, the understanding of the device behavior and verification of compact models for such applications should be done based on the discussed FOM.

3 SUMMARY

This paper discusses important device parameters to be used as FOM in evaluating technology performance and qualifying device models for analog/RF applications. They should be used in the future to guide the process technology development and qualify the device models targeted for analog/RF applications. Model developers should always keep these FOM in minds while they focus on modeling work. In particular, the modelers, who generate models for circuit designers for specific RF applications, should validate the models against most of these FOM, if not all, to ensure the model function properly in predicting device behavior at HF.

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