Correlated Noise Modeling and Simulation

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ABSTRACT

This paper addresses several issues in noise modeling and simulation. It shows how correlated noise can be implemented in Verilog-A, and presents a new and simple technique to simulate the noise correlation coefficient using only the standard Spice noise analysis. An analytic proof is given that the noise contributed by the distributed gate resistance of a MOSFET can be modeled by including a resistance of value $R_g/3$ in series with the gate capacitance, which serendipitously provides good low frequency AC modeling. Analysis of series and parallel combinations of devices is done to derive fundamental geometric scaling relations for noise. Finally, implementation of correlated MOSFET gate in Verilog-A is demonstrated, and it is shown that the gate noise must be distributed between gate-source and gate-drain components to maintain proper symmetry.

Keywords: Noise modeling, noise simulation, Verilog-A, MOSFET noise, noise correlation.

1. INTRODUCTION

Circuit simulation for IC design normally brings to mind DC, AC, and transient circuit analysis. For RF communications circuits, non-linearity and noise are key figures of merit that must be simulated, and there has been significant effort in the past years to improve models and simulation algorithms for such analyses. This paper addresses topics in noise modeling and analysis.

2. CORRELATED NOISE IN VERILOG-A

Over the past several years Verilog-A has emerged as the preferred language for writing compact models [1][2], and the latest version of the Verilog-A language was specifically driven by the need to add constructs to support its burgeoning use to define compact models [3]. Although Verilog-A includes the noise functions `white_noise()`, `flicker_noise()`, and `noise_table()`, and the LRM includes an example of how to implement correlated noise (with a real valued correlation coefficient), there has been on-going questioning of whether Verilog-A has sufficient capability to allow proper modeling of correlated noise for MOSFETs. In part this is because (in saturation) the correlation coefficient between gate and drain noise currents is imaginary ($j\sqrt{5/32}$, [4] p. 90). This perception may also in part be due to the fact that handling of noise by Verilog-A compilers appears to be in a less mature state than handling of other parts of the language.

Correlated noise, including an imaginary (or arbitrary complex) correlation coefficient, can be implemented in Verilog-A, as Fig. 1 shows.

```
`include "discipline.h"
`include "constants.h"
module correlatedNoise2Port(n1,n2);
inout      n1,n2;
electrical n1,n2;
electrical ia,ib;
parameter  real c   = 0.0 from [0:1];
parameter  real ang = 0.0 from [0:360];
real cr, ci, cbar;
analog begin
cbar = sqrt(1.0-c*c);
cr   = c*cos((ang/180.0)*`M_PI);
ci   = c*sin((ang/180.0)*`M_PI);
I(ia)<+white_noise(4*`P_K*$temperature);
I(ib)<+white_noise(4*`P_K*$temperature);
I(ia)<+V(ia);
I(ib)<+V(ib);
I(n1)<+V(n1)+   V(ia);
I(n2)<+V(n2)+cr*V(ia)+cbar*V(ib);
I(n2)<+ ddt(-ci*V(ia));
end
endmodule
```

Fig. 1 Generic Noise Correlation in Verilog-A

The model of Fig. 1 is a two port, with implicit ground reference, and for DC and AC consists of a 1 Ohm resistor from each port to ground. The parameters `c` and `ang` are the magnitude and phase of the correlation between the noise currents in the two ports. The internal nodes `ia` and `ib` are used to generate independent noise contributions (equivalent to the thermal noise of 1 Ohm resistors), and then weighted combinations of these noises are added to the port currents. It is the adjustment of the weighting that allows arbitrary degrees of correlation to be implemented.

Note that the internal nodes `ia` and `ib` include contributions equivalent to 1 Ohm resistors. This ensures these nodes are not floating, and converts the noise currents into noise voltages, whose numerical voltage values are the noise currents, on the nodes `ia` and `ib`.

If `c=0` then `cr=ci=0` and `cbar=1` and clearly the noise currents in ports 1 and 2 are independent and uncorrelated. If then `c=1` then `cbar=0` and clearly the noise currents in ports 1 and 2 are perfectly correlated. The

`ddt()` operator induces a 90 degree phase shift that leads to the imaginary component of the correlation. This also makes the imaginary noise component of `I(n2)` vary as ω^2, which is to be expected as imaginary noise correlation arises from capacitive coupling. The negative sign for this contribution is required as the correlation coefficient is defined using the conjugate of the port 2 noise current.

Note that the above example needs modification if the "base" noise magnitudes are different, and that the magnitude of the noise in port 2 varies with frequency. Nevertheless, it shows the basics of how to implement correlated noise: generate independent noise sources and combine in ratioed parts to implement real correlation, use the `ddt()` operator to implement imaginary correlation (with an ω^2 frequency dependence).

3. SPICE SIMULATION OF NOISE CORRELATION

Some simulators allow definition of multiports, and simulate complete small-signal multiport matrices for them, including noise currents and cross correlations. However, not all circuit simulators have this capability. A 15 step procedure to extract gate and drain noise, and their correlation, for MOSFETs was presented in [5]. If this procedure was applied to simulations the de-embedding steps could be omitted, but it is still a somewhat complex process.

Is there a simple way to calculate noise correlations using the standard SPICE noise analysis [6]? Because noise is a statistical process and standard noise analysis deals in square quantities, the answer to this question turns out to be yes. Consider adding two noise currents, for convenience taken to be of equal magnitude i_n^2 A^2/Hz. If the noise currents are uncorrelated then the total noise current is $2i_n^2$. However, if the noise currents are perfectly correlated then the summed noise current is $4i_n^2$. Sums (and differences) of currents are easy to generate in SPICE using controlled sources, and these can be used to compute both real and imaginary correlations between noise currents.

Let i_1 and i_2 be the port currents of a 2-port network (strictly we should be working in terms of noise current spectral density, but the analysis is at one frequency so we will just refer to noise currents for simplicity). Consider these currents to be formed from independent noise sources i_a and i_b and a complex correlation $\chi = \chi_r + j\chi_i$, as in the example of Fig. 1,

(1) $i_1 = i_a$

(2) $i_2 = (\chi_r + j\chi_i)i_a + \sqrt{1-\chi^2}\,i_b$

where $\chi^2 = \chi_r^2 + \chi_i^2$. Using controlled sources, and a capacitor to implement a $\pi/2$ phase shift, form the quantities

(3) $i_p = i_1 + i_2,\ i_m = i_1 - i_2,\ i_{pj} = i_1 + ji_2,\ i_{mj} = i_1 - ji_2$.

The squared noises of each of these quantities, which is what SPICE reports for a standard noise analysis, are

(4) $i_1^2 = \overline{i_1 i_1^*} = i_a^2$

(5) $i_2^2 = \overline{i_2 i_2^*} = \chi^2 i_a^2 + \left(1-\chi^2\right) i_b^2$

(6) $i_p^2 = \overline{i_p i_p^*} = \left((1+\chi_r)^2 + \chi_i^2\right) i_a^2 + \left(1-\chi^2\right) i_b^2$

(7) $i_m^2 = \overline{i_m i_m^*} = \left((1-\chi_r)^2 + \chi_i^2\right) i_a^2 + \left(1-\chi^2\right) i_b^2$

(8) $i_{pj}^2 = \overline{i_{pj} i_{pj}^*} = \left((1-\chi_i)^2 + \chi_r^2\right) i_a^2 + \left(1-\chi^2\right) i_b^2$

(9) $i_{mj}^2 = \overline{i_{mj} i_{mj}^*} = \left((1+\chi_i)^2 + \chi_r^2\right) i_a^2 + \left(1-\chi^2\right) i_b^2$.

The correlation coefficient between i_1 and i_2 is

(10) $c = c_r + jc_i = \dfrac{\overline{i_1 i_2^*}}{\sqrt{\overline{i_1 i_1^*}\;\overline{i_2 i_2^*}}} = \dfrac{(\chi_r - j\chi_i) i_a^2}{\sqrt{i_a^2\left(\chi^2 i_a^2 + \left(1-\chi^2\right) i_b^2\right)}}$

and comparison with the sum and difference terms gives

(11) $c_r = \dfrac{i_p^2 - i_m^2}{4\sqrt{i_1^2 i_2^2}}$

(12) $c_i = \dfrac{i_{pj}^2 - i_{mj}^2}{4\sqrt{i_1^2 i_2^2}}$.

Numerical simulations on a distributed MOSFET model, and comparison with a 2-port noise analysis, verified that this approach works. Also, values of `c` and `ang` fed into the model of Fig. 1 were exactly extracted based on simulations using the approach.

The only unsavory aspect of this technique is that a separate analysis must be run for each frequency. The $\pi/2$ phase shift is implemented with a capacitor, whose admittance is $j\omega C$ and hence whose value C must be $1/\omega$, and so is set separately for each frequency.

4. DISTRIBUTED RC NOISE

In [7] it is shown that using the standard $\rho_{gsh}W/3LN_C^2$ value for gate resistance (where N_C is the number of gate connections, 1 or 2), which is known to provide AC modeling that matches the first order expansion of the transmission line model for the distributed gate resistance and capacitance system, also provides correct modeling of the gate (and drain) noise currents. Simulations of a distributed RC system (with a contact on one end only) by a multi-section model also shows that as the number of

sections increases the (gate) noise current converges to that of a resistor of value $R/3$ in series with a capacitance C.

In [8] there is an elegant analysis of the effect of distributed gate resistance on MOSFET performance, including noise. Drain current noise is considered, and it is shown that including a lumped $R_g/3$ in series with the gate gives drain current noise that matches multi-section simulations. However, as pointed out in [7], the analysis of [8] does not consider gate current noise.

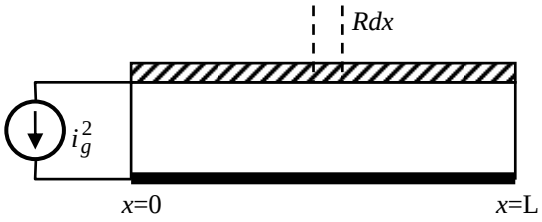

Fig. 2 Distributed RC Analysis of Gate Resistance

Consider the distributed RC system of Fig. 2, where we consider the gate resistance effect but assume that the channel is highly conducting, so we are only interested in the effect of the gate resistance. The analysis is for a gate contact on one side, and we need to determine the noise current flowing in the AC short circuit on the left side of the figure. Associated with the element of length dx is a series noise voltage source of magnitude $4kTRdx/L$ (V^2/Hz). Analysis of the transmission line matrices for the sections to the left and right of the elemental section, to calculate the transformation from the noise voltage of the element dx to the noise current in the gate connection, shows that it is dominated (at low frequencies) by the admittance $j\omega C(1-x/L)$ to the right of the element dx. This makes sense because the admittance of the left portion is dominated by the conductance of the gate resistance, and this is (at low frequencies) much less than the admittance of the gate capacitance to the right of the element. Therefore, the gate noise current is, to first order, determined by the noise voltage $4kTRdx/L$ in series with a capacitance $C(1-x/L)$. Integrating this over the whole device gives

$$(13)\quad i_g^2 = \int_0^L \omega^2 C^2 (1-x/L)^2 (4kTR/L)\,dx = 4kT\omega^2 C^2 R/3.$$

This is exactly equivalent to the gate noise from a series combination of a resistance $R/3$ and a capacitance C, in agreement with the results of multi-section simulations.

For contacts at both ends of the gate, symmetry considerations dictate the factor $1/3$ be replaced by $1/12$.

5. Restrictions on Geometry Scaling of Noise

Many forms for noise models for semiconductors have been proposed, e.g. for resistors (including both thermal and $1/f$ noise components) [9]

$$(14)\quad S_i = 4kTG + K_F \frac{I^2}{WL}\frac{1}{f},$$

for MOSFET thermal noise [10]

$$(15)\quad S_{i,th} = 4kT\frac{\mu|Q_i|}{L^2},$$

and for MOSFET $1/f$ noise [10][11]

$$(16)\quad S_{i,1/f} = \frac{K_F I_d^{A_F}}{C_{ox}L^2 f}, \frac{K_F I_d^{A_F}}{C_{ox}^2 WLf}, \text{ or } \frac{K_F g_m^{A_F}}{C_{ox}WLf}.$$

Often exponents (of current or transconductance, geometry, and frequency) in the above expressions are cast as model parameters that can be adjusted to give the best fit of the model to data, typically from only one or a small number of geometries. It is known that this can lead to incorrect scaling of noise with geometry.

The question then is: what physical restrictions need to be applied to noise model formulations? Physically, if a device of length L and width W is considered as two devices of length L and width $W/2$ in parallel, or two devices of length $L/2$ and width W in series, then the noise should be the same. (This assumes that the current density and noise sources in a device are spatially uniform, that the current flows in the length direction, that the noise sources are spatially uncorrelated, and short and narrow device effects are ignored.)

Assume that the noise current spectral density is

$$(17)\quad S_i \propto X^a W^b L^c$$

where X is either resistor or MOSFET current or MOSFET g_m (in nonsaturation), and the device is biased with a voltage source and so is driving an AC short circuit load.

For the case of two $W/2$ devices in parallel, for each half width device X is also halved, therefore the total noise current from the two halves is $2(X/2)^a (W/2)^b L^c$ and this is equal to (17) only if $b = 1-a$.

Similarly, for the case of two $L/2$ devices in series, each half length device contributes $X^a W^b (L/2)^c/4$ to the total output noise current (current or non-saturation g_m is independent of length, and the factor 1/4 arises because 1/2 the noise current from one section flows in the external AC short, where we are measuring the noise current, and this factor is squared as we are considering the spectral density in A^2/Hz). Summing the contributions from each segment and equating to (17) implies that $c = -1$.

Therefore, basic physical considerations require that

$$(18)\quad S_i \propto \frac{X^a}{LW^{a-1}}$$

must hold (although this can be modified for short and narrow device effects, it must hold asymptotically for large devices). Note that there is no assumption about the type of noise (thermal or $1/f$), and (18) is valid for all noise types.

Thermal noise is independent of current, and therefore from (18) must vary as W/L. Clearly this is true for the thermal component of (14) and, as $Q_i \propto LW$, for (15).

The first form in (16) is obviously incorrect, as is widely known, and the reason for the incorrect scaling with geometry when $A_F \neq 2$ of the other two forms is apparent. Although it seems intuitive that $1/f$ noise should scale inversely with device area, and so adding flexibility in noise modeling over bias by making only the exponent of the bias dependent term variable seems reasonable, this breaks the asymptotic geometric scaling of noise.

For devices like BJTs and diodes, where currents scale with area A and not W/L ratio, a similar analysis (assuming the noise varies as some power of current) gives

$$(19)\quad S_i \propto \frac{I^a}{A^{a-1}}$$

(and an equivalent form holds for perimeter components). It is common for BJT $1/f$ noise models to vary with base current I_b as $I_b^{A_F}/WL$ but (19) shows that the commonly assumed inverse area dependence needs to be adjusted if $A_F \neq 2$. This is in fact the case for SPICE diode models, which by default have $A_F = 1$ [11]. Experimental evidence supports $A_F = 2$ for diodes [12], and using a derivation based on current density the relation (19) has been noted previously for BJTs [13]; in [13] the observed I_b^2 dependence of $1/f$ noise was noted as evidence that the underlying noise sources are spatially uniform and uncorrelated.

6. MOSFET Induced Gate Noise Implementation in Verilog-A

MOSFET induced gate noise is naturally simulated by using a sectional MOSFET model [7]. An expression for the magnitude of the induced gate noise is given in [14]; here we show how to implement MOSFET gate noise in Verilog-A to capture both the magnitude and the correlation to the drain noise.

As a reference (long-channel) model we use the symmetric bulk charge linearization model of [15], with a simple regional surface potential model and the thermal noise model (15) from [10]. Simulations were done of up to 50 section models, over bias and frequency. These showed that the important characteristics of the drain and gate noise currents, and their correlation, were apparent in plots versus frequency at $V_{ds} = V_{gs} = 2.5$ (the device is operating in saturation at that bias), and in plots versus V_{ds} at $V_{gs} = 2.5$ and $f = 100$ MHz (which is below the device f_T of about 20GHz).

Simulations over a wide range of geometries, biases, and physical parameters shows that (at a given frequency below f_T)

$$(20)\quad \frac{S_{i_g}}{S_{i_d}} \propto \frac{L^4}{\mu^2 q_i^2}$$

where $q_i = Q_i/LWC_{ox}$ is the normalized inversion charge, and the proportionality constant is about 1/13 (this leads to the same form for S_{i_g} as given in [14]). As is well known, S_{i_g} varies as ω^2, and in saturation the correlation coefficient between gate and drain noise currents is [4]

$$(21)\quad c = \frac{\overline{i_g i_d^*}}{\sqrt{S_{i_g} S_{i_d}}} \approx 0.395j$$

and hence using the technique introduced in section 2 to implement correlated noise in Verilog-A, it should be possible to implement correlated gate noise for a MOSFET model using only a single element (not a multi-section) model.

Introducing an internal node `n` at which to generate the noise current component that is correlated between gate and drain, it would seem that the simplest way to do this is via something like (full details of declarations are omitted for brevity):

```
parameter real ci    = 0.3987;
parameter real ratio = 0.2755;
real sid, sigrat, qi;
sid   =(4.0*`KB*tdevK*mu0*(qi*W*cox)/L);
sigrat=ratio*L*L/(mu0*qi);
I(d,s)<+white_noise((1.0-ci*ci)*sid);
I(n)  <+V(n);
I(n)  <+white_noise(sid);
I(d,s)<+ci*V(n);
I(g,s)<+ddt(V(n)*sigrat);
```

Fig. 3 Simple Induced Gate Noise in Verilog-A

Here `qi` is the (absolute value of the) normalized inversion charge, and so is multiplied by LWC_{ox} to generate the Q_i of (15). The imaginary correlation `ci` was set to 0.3987 rather than 0.395 as this led to better matching to multi-section simulations, and the parameter that controls the ratio of gate to drain noise, `ratio`, was also empirically adjusted to optimize the fit of the single element model to results from (50 segment) distributed simulations. The other variables have obvious meanings, and note that the square root of the ratio (20) is used as the noise analysis squares the effect of scale factors.

Although the code snippet of Fig. 3 does simulate induced gate noise, and has the correct magnitude and correlation to the drain noise (in saturation, at frequencies below f_T), it has one subtle problem: it is not properly symmetric. As a device goes from non-saturation to

saturation operation (as V_{ds} increases), C_{gs} increases and C_{gd} decreases, therefore the gate noise current should become more associated with a gate-source than gate-drain component. Introducing a partitioning of the gate noise current based on the relative magnitudes of the components of inversion charge associated with the source and drain nodes respectively (q_s and q_d), leads to

```
parameter real ci    = 0.3987;
parameter real ratio = 0.2755;
real sid, sigrat, qi, qs, qd;
sid   =(4.0*`KB*tdevK*mu0*(qi*W*cox)/L);
sigrat=ratio*L*L/(mu0*qi);
I(d,s)<+white_noise((1.0-ci*ci)*sid);
I(n)  <+V(n);
I(n)  <+white_noise(sid);
I(d,s)<+ci*V(n);
I(g,s)<+ddt(V(n)*sigrat*qs/qi);
I(g,d)<+ddt(V(n)*sigrat*qd/qi);
```

Fig. 4 Symmetric Induced Gate Noise in Verilog-A

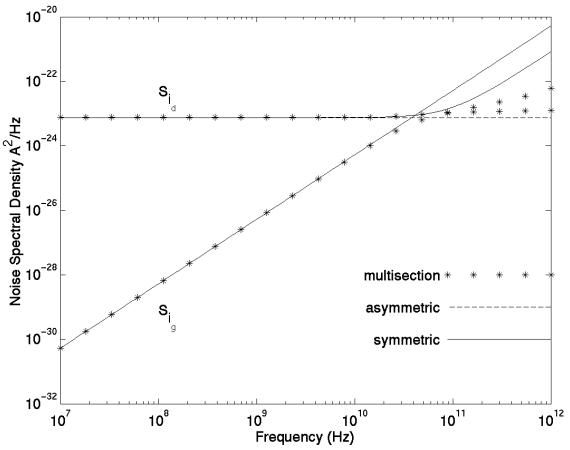

Fig. 5 Drain and Gate Noise vs. Frequency, in Saturation.

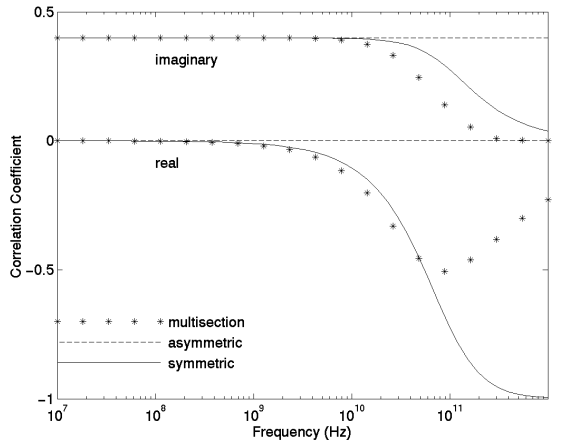

Fig. 6 Noise Correlation vs. Frequency, in Saturation

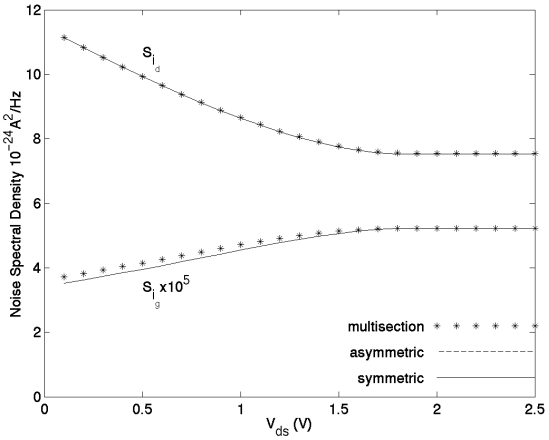

Fig. 7 Drain and Gate Noise vs. V_{ds} , f=100MHz

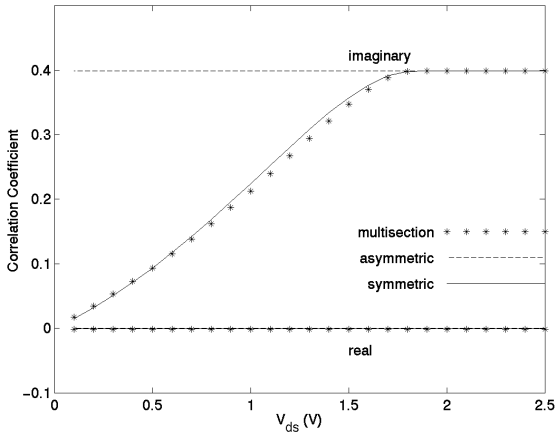

Fig. 8 Noise Correlation vs. V_{ds} , f=100MHz

Comparisons of simulations from the above two models with a reference simulation from a 10-section distributed model (with no explicit implementation of correlated gate noise, as in [7]) are shown in Fig. 5 through Fig. 8, for the bias conditions specified above.

The noise currents as a function of drain bias (Fig. 7) match well because of the accuracy of the charge calculations of the model of [15]. The single section model diverges from the multi-section simulations at high frequencies in Fig. 5 and Fig. 6, but these are at or beyond the f_T of the device.

Note that in Fig. 8 the symmetric induced gate noise model of Fig. 4 includes an additional factor for the correlation coefficient, which is a function of $q_s - q_d$, that causes the correlation to go to zero at $V_{ds} = 0$, otherwise the curve in Fig. 8 for the symmetric model matches that for the asymmetric model.

An interesting feature, seen in Fig. 6, is that the introduction of symmetric gate-source and gate-drain components of the gate noise current has the serendipitous side benefit of introducing a frequency dependence into the correlation coefficient that at least qualitatively matches the

reference multi-section simulation up to the frequency where there is an extreme of the real part of the correlation coefficient, about $5f_T$. The distinguishing characteristics of the single and multi-section models at high frequency have the hallmarks of lumped element versus distributed models for AC behavior.

Note that the above simulations are for ideal long channel behavior, experiment shows that the correlation coefficient between gate and drain noise decreases as the channel length decreases [5][7].

7. CONCLUSIONS

Noise modeling and simulation are important for analog and mixed-signal ICs. This paper has reviewed some existing and new results in noise modeling and simulation. It has given an example of how correlated noise, including imaginary correlation, can be implemented in Verilog-A, and has used this to implement correlated gate noise in a simple, yet reasonably accurate, MOSFET model. To our knowledge, this is the first time correlated noise, including an imaginary component, implemented in Verilog-A has been reported.

Simulation and extraction of noise correlation can be difficult, and we have shown how forming simple sums and differences of currents allows noise correlation to be extracted from normal SPICE noise simulations, which only provide total squared noise currents. This obviates the need for special *s*-parameter or multi-port analyses to allow simulation of noise correlation.

We also provide an analytic verification of the observation, from distributed simulations, that the gate noise from gate resistance, for a one-sided contact, is properly modeled (at frequencies below the corner frequency of the distributed RC system) by including a resistance of $R_g/3$ in series with the gate capacitance. Fortunately this is the same value needed to match low frequency AC performance.

Finally, we have derived restrictions on the bias and geometry dependence of some forms of noise models, that must be met asymptotically for large geometries. These restriction follow directly from the equivalence of one device to two half (length or width) devices (in series or parallel).

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We would like to thank J. Victory for pointing out that the g_m of a MOSFET in nonsaturation is proportional to longitudinal field, therefore the analysis of section 5 is applicable in that case as well as for resistors. We would also like to thank B. Gu for setting up initial simulations to verify the technique of section 3, and Wladek Grabinski for discussions on the modeling and simulation of noise correlation.

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