Introduction to PSP MOSFET Model (Invited)

G. Gildenblat, X. Li, H. Wang, W. Wu
Department of Electrical Engineering
The Pennsylvania State University, University Park, USA
and
R. van Langevelde, A.J. Scholten, G.D.J. Smit and D.B.M. Klaassen
Philips Research Laboratories, Prof. Holstlaan 4 (WAY41), 5656 AA Eindhoven, The Netherlands

ABSTRACT

PSP is the latest and the most advanced compact MOSFET model developed by merging the best features of the two surface potential-based models: SP (developed at The Pennsylvania State University) and MM11 (developed by Philips Research). This work presents the main ideas enabling the development of PSP, model structure and its general features. Comparison with experimental data and simulation examples are included as well.

Keywords: compact model, MOSFET, surface potential

1 INTRODUCTION

There is presently a wide consensus in the compact modeling community that traditional threshold-voltage-based models of MOS transistors have reached the limit of their usefulness and need to be replaced with the more advanced surface-potential- based or inversion charge-based models (we use model classification suggested in [1]). The development of compact MOSFET models at Philips [2, 3] and at The Pennsylvania State University [1, 4–6] has followed the surface-potential-based approach in order to provide the physics-based modeling of all regions of operation and not to make additional approximations beyond those that are already inherent in the charge-sheet models. Indeed, while the constitutive equation of the inversion-charge-based models can be derived differently, in the final analysis it follows from the equation for the surface potential in which the accumulation region is neglected and the bulk charge is eliminated using an additional approximation [1]. Another motivation for the selection of the surface-potential-based approach is that it enables the physical modeling of the source-drain overlap regions where the inversion charge is not a particularly suitable variable.

The surface-potential-based approach to modeling MOS transistors dates back to the Pao-Sah [7]. The modern surface-potential-based models are based on the charge-sheet model (CSM) of Brews [8]. Despite the clear physics and the ability to provide a single expression for all regions of operation [9] surface-potential-based models did not become popular until the last decade due, in part, to their perceived complexity. Successful surface-potential-based models became possible only after significant progress was made in the techniques for the computing the surface potential, simplification of the charge equations relative to the original formulation ("symmetric linearization" method [5, 6]) and the introduction of small-geometry effects.

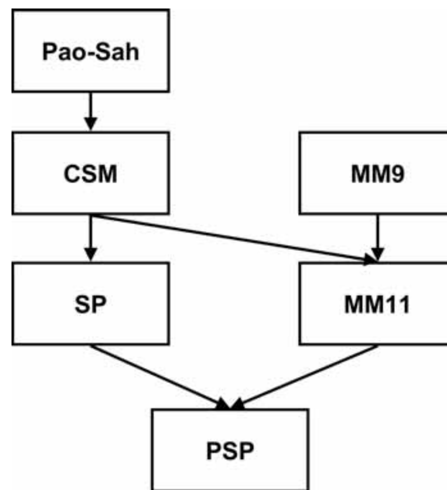

Figure 1: Origin of PSP

The implementation of these advances and the overall model structures of SP [1] and MM11 [2] turned out to be compatible, enabling the merger of both models into a single new model called PSP (Fig. 1) that combines the best features of SP and MM11. This paper provides an overview of PSP.

2 GENERAL FEATURES OF PSP

The model structure shown in Fig. 2 consists of the core and enhancement blocks. The core block contains the quasi-static (QS) intrinsic and the extrinsic models. The intrinsic model contains expressions for the drain current, terminal charges and the noise sources. The extrinsic model includes contributions of the source-drain overlap regions, gate and substrate currents, etc. The enhancement block contains junction model developed using [10] as a starting point and the NQS module [6, 11].

Both MM11 and SP distinguish between local and global model parameters. This approach is carried over to PSP. Global parameters include geometry dependences and before evaluating MOSFET output characteristics are converted into a small number (about 35) of local parameters actually used in the core model. One possible approach to the model parameter extraction is to extract the local parameters ("miniset") for each device geometry and then to use scaling equations to obtain the global parameters ("maxiset") for the relevant range of geometries. The actual local parameters used in circuit

simulations are then recomputed from the global parameters.

The major features of PSP include the following.

- Physical surface-potential-based formulation in both intrinsic and extrinsic model modules
- Physical and accurate description of the accumulation region
- Inclusion of all relevant small geometry effects
- Modeling of the halo implant effects, including the output conductance degradation in long devices
- Coulomb scattering and non-universality in the mobility model
- Non-singular velocity-field relation enabling the modeling of RF distortions including intermodulation effects (IM3)
- Complete Gummel symmetry
- Mid-point bias linearization enabling accurate modeling of the ratio-based circuits (e.g. R2R circuits)
- Quantum-mechanical corrections
- Correction for the polysilicon depletion effects
- GIDL/GISL model
- Surface-potential-based noise model including channel thermal noise, flicker noise and channel-induced gate noise.
- Advanced junction model including trap-assisted tunneling, band-to-band tunneling and avalanche breakdown
- Spline-collocation-based NQS model including all terminal currents
- Stress model

3 MOBILITY

The mobility expression used in PSP is given by

$$\mu = \frac{\mathrm{MU0} \cdot \mu_x}{1 + (\mathrm{MUE} \cdot E_{eff})^{\mathrm{THEMU}} + \frac{\mathrm{CS} \cdot q_{bm}^2}{(q_{bm}+q_{im})^2} + \rho} \quad (1)$$

where MU0 is the low-field mobility, parameters MUE and THEMU account for the mobility degradation by the effective vertical field, E_{eff}, Coulomb scattering is introduced as in [12] using the parameter CS, q_{bm} is the bulk charge per unit channel area at the surface potential midpoint [1], q_{im} is the density of the inversion charge also at the potential midpoint and the factor μ_x describes the non-universality effects and also accounts (empirically) for the doping non-uniformity. The factor ρ accounts for the series resistance and is set to zero when the latter is included externally.

4 VELOCITY SATURATION

Velocity saturation is critical not only for the accurate modeling of the saturation region but also to insure the nonsingular behavior of the model at zero drain bias [13,14]. The saturation velocity model used in PSP is that of MM11 [2]. For n-channel devices

$$V_d = \frac{\mu E_y}{\sqrt{1 + (E_y/E_c)^2}} \quad (2)$$

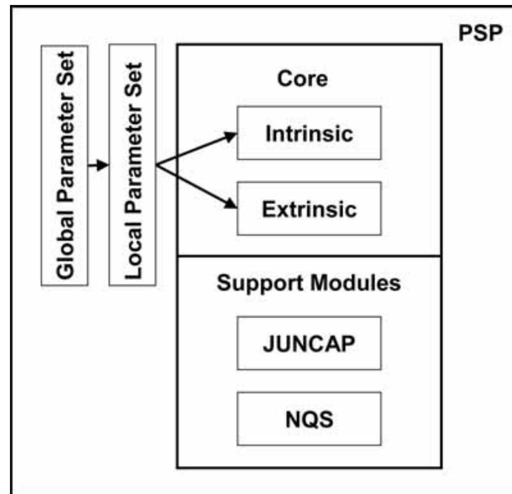

Figure 2: Structure of PSP Model

where E_c denotes the critical field and E_y is the lateral component of the electric field. In terms of the drain current this leads to an expression

$$I_d = \frac{2\mu\,(W/L)\,q_{eff}\Delta\psi}{1 + \sqrt{1 + 2\,(\Delta\psi/E_c L)^2}} \quad (3)$$

where $\Delta\psi$ is the surface potential difference across the channel and q_{eff} is the effective inversion charge density modified to account for the diffusion current component.

Similar expressions are adopted for p-channel devices with suitable modifications to account for the difference in the shape of the velocity-field relation for holes and electrons in silicon. These expressions are non-singular enabling, for example, the modeling of passive RF mixers first accomplished in SP using a somewhat different approach [14]. As shown in [15] they also enable accurate modeling of RF distortions in the saturation region.

5 LATERAL FIELD GRADIENT FACTOR

To extend the model formulation beyond the gradient channel approximation PSP relies on the lateral gradient factor introduced in [16]:

$$f = 1 - (\varepsilon_s/qN_{sub})\,\partial^2\psi_s/\partial y^2 \quad (4)$$

where ε_s is the absolute dielectric constant of silicon and N_{sub} denotes the substrate doping. The initial application of this method of modeling short-channel effects used the approximation $f = f(L, W)$ [17], but in PSP as in SP [1] we use a bias-dependent approximation for f. The expression for f in PSP is modified relative to SP to account for the experience gained in using the lateral gradient factor for the purpose of compact modeling.

6 SYMMETRIC LINEARIZATION

The key to the merger of SP and MM11 is inclusion of expressions (2) and (3) within the context of symmetric linearization. The initial version of this technique was developed for long-channel devices to verify

the concept, but its implementation in SP includes velocity saturation described via the Grotjohn-Hofflinger method [18, 19]. The explicit form of the surface position dependence in the symmetric linearization method is given by

$$\psi(y) = \psi_m + H\left[1 - \sqrt{1 - \frac{2\Delta\psi}{HL}(y - y_m)}\right] \quad (5)$$

where the coordinate y is measured from the source towards the drain end of the channel, ψ_m is the average surface potential in the channel, and y_m denotes the coordinate of the surface potential midpoint (a point where the surface potential ψ equals ψ_m):

$$y_m = \frac{L}{2}\left(1 + \frac{\Delta\psi}{4H}\right) \quad (6)$$

To clarify the exposition of major concepts (5), all subsequent equations are written without the channel length modulation factor. The complete set of PSP equations will be presented elsewhere. In the long-channel version of the symmetric linearization method [5]

$$H_0 = (q_{im}/\alpha) + \phi_t \quad (7)$$

where $\phi_t = kT/q$ is the thermal potential, q_{im} is the inversion charge density at the potential midpoint and α denotes the linearization coefficient in the expression [1, 5]

$$q_i = q_{im} - \alpha(\psi_s - \psi_m) \quad (8)$$

for the inversion charge density. The relation between q_{im} and q_{eff} is as follows

$$q_{eff} = q_{im} + \alpha\phi_t \quad (9)$$

The flexibility of the symmetric linearization method is such that eqs. (5), (6) remain unchanged when the velocity saturation is included, the only difference being the change in the expression for H [1]:

$$H_{\mathrm{SP}} = H_0\left(1 + \delta_0\Delta\psi/E_cL\right)^{-1} \quad (10)$$

where δ_0 is a bias-dependent variable introduced to account for the details of the velocity-field relation [18] and to remove the singularity at $V_{ds} = 0$ [14].

This approach is carried over to PSP where the position dependence of the surface potential is still given by (5) but in order to accommodate the different expression for the drift velocity and the drain current, instead of (10) we set

$$H_{\mathrm{PSP}} = q_{eff}/\alpha' h \quad (11)$$

where

$$\alpha' = \alpha\left[1 + \frac{1}{2}\left(\frac{\Delta\psi}{hE_cL}\right)^2\right] \quad (12)$$

and

$$\mathrm{h} = \frac{1}{2} + \frac{1}{2}\left[1 + 2\left(\frac{\Delta\psi}{E_cL}\right)^2\right]^{\frac{1}{2}} \quad (13)$$

With this in mind the quasi-static terminal charges can be evaluated as in [1, 5], and [6] with the only difference being that now $H = H_{PSP}$. For example, the

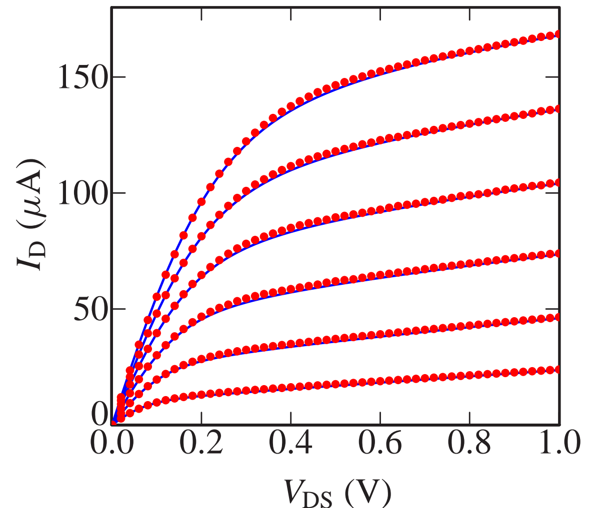

Figure 3: Output characteristics of 0.36/0.09μm MOSFET; V_{gs} varies between 0.5 and 1V, V_{sb}=0. Circles represent measured data, solid lines correspond to PSP

normalized drain charge given in the Ward-Dutton partition [20] by the integral

$$Q_D = \frac{1}{L}\int_0^L \frac{y}{L} q_i dy \quad (14)$$

becomes

$$Q_D = \frac{q_{im}}{2} + \frac{\alpha\Delta\psi}{12}\left(1 - \frac{\Delta\psi}{2H_{PSP}} - \frac{\Delta\psi^2}{20H_{PSP}^2}\right) \quad (15)$$

The expressions for the current and terminal charges obtained in this manner are continuous and smooth in all regions of operation from accumulation to deep inversion. The linearization scheme adopted in PSP (as well as those in SP and MM11) enables accurate modeling of ratio-based circuits. A detailed discussion including applications to R2R circuits can be found in [21].

7 EXPERIMENTAL VERIFICATION

Comparison of PSP with experimental data was performed using data from the 90nm CMOS technology node. The results presented below are for a 0.36μm/90nm device. Due to space limitations global PSP fits will be presented elsewhere. As shown in Figs. 3-5 an excellent fit of the device characteristics is obtained in all regions of operation.

The inclusion of short-channel and narrow-channel effects in PSP is sufficiently flexible to allow an accurate description of the device output conductance including the case of low gate drive (cf. Fig. 5). The physical nature of PSP is responsible for the excellent reproduction of the g_m/I_d characteristics shown in Fig. 6 and important for analog and mixed applications of the model.

The availability of the surface potential both in the active and the source/drain overlap regions of the device enables the use of the surface-potential-based gate current model developed in [22, 23] and adapted to PSP by

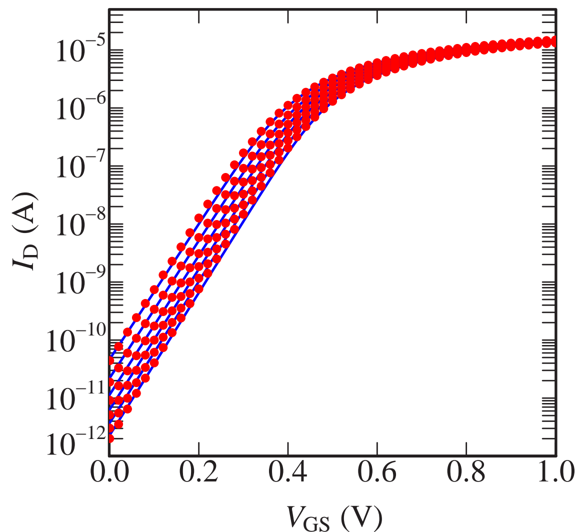

Figure 4: MOSFET transfer characteristics; V_{ds}=25mV, V_{sb}=0, 0.2...1.0V

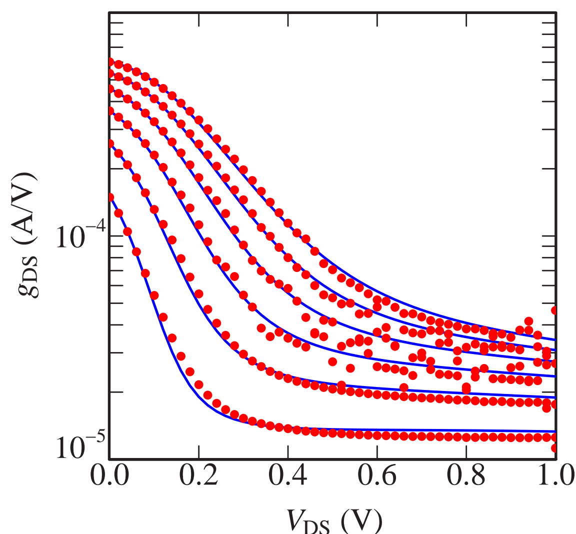

Figure 5: Output conductance; V_{gs} varies between 0.5 and 1V, V_{sb}=0

changing parameter H in the channel region as described in the previous section. Comparison with experimental data is presented in Fig. 7 and indicates the high degree of accuracy. The same technique is used to model the contributions of the overlap regions to the capacitance-voltage characteristics [24, 25]. Typical CV curves are shown in Fig. 8, 9.

8 NOISE MODEL

PSP includes $1/f$ noise, channel thermal noise and induced gate noise. The PSP flicker noise model is obtained by developing a surface-potential-based version of the general model in [26], which combines both carrier numbers and mobility fluctuations. This formulation improves an earlier version of the surface-potential-based adaption of [26] given in [2, 25]. For the channel thermal noise and the induced gate noise, PSP makes use of the improved Klaassen-Prins approach introduced in [27], where fluctuations in the velocity saturation term are also taken into account. Using the symmetric linearization scheme, the improved approach is developed in the ψ_s-framework. The resulting noise model has been verified down to the 90nm CMOS technology node, see Fig. 10. The model is in good agreement with measurement data without using any additional noise parameters.

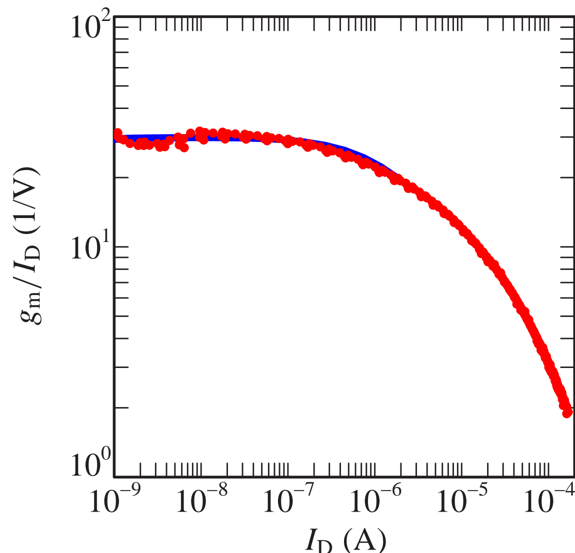

Figure 6: g_m/I_d characteristics; V_{ds}=1V, V_{sb}=0V, V_{gs} varies continously between 0 and 1V, V_{sb}=0, 0.2...1.0V

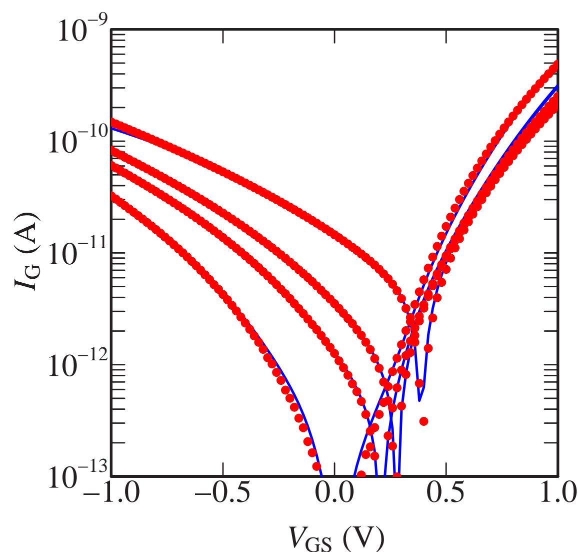

Figure 7: Gate tunneling current; V_{sb}=0V, V_{ds}=0.025, 0.042, 0.61 and 1V

9 NON-QUASI-STATIC MODEL

The modeling of fast transients and high-frequency small-signal characteristics of the MOSFET often requires an NQS model of the device. Of the several NQS techniques available at the present time, two al-

NSTI-Nanotech 2005, www.nsti.org, ISBN 0-9767985-3-0 WCM, 2005

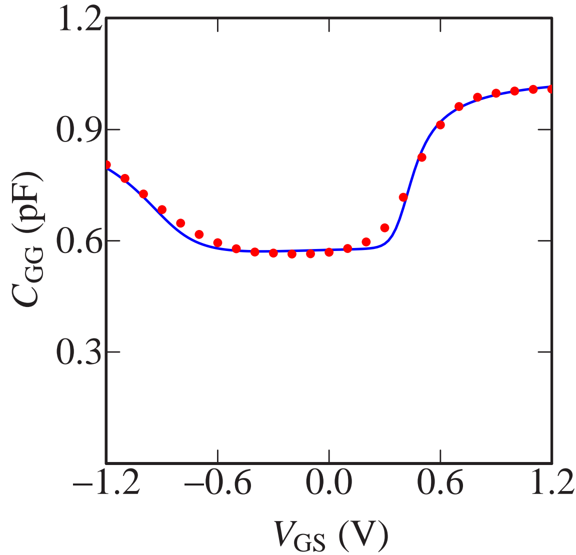

Figure 8: Measured (symbols) and modelled (lines) input capacitance C_{gg} as a function of gate bias V_{gs} for W/L=800μm/90nm n-channel MOSFET; V_{ds}=0, V_{sb}=0

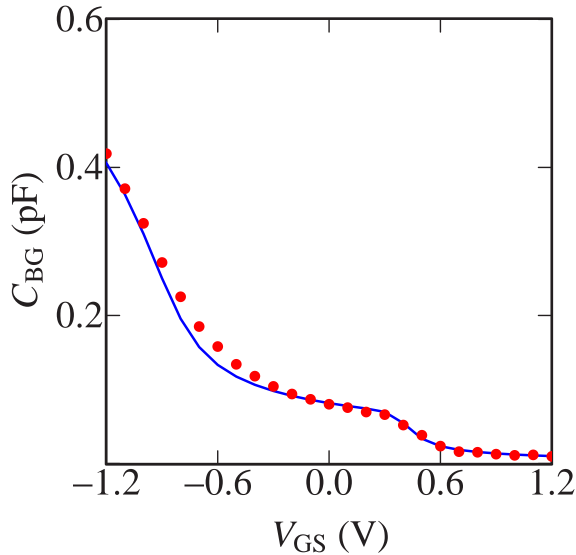

Figure 9: Measured (symbols) and modelled (lines) transcapacitance C_{bg} as a function of gate bias V_{gs} for W/L=800μm/90nm n-channel MOSFET; V_{ds}=0, V_{sb}=0

low an arbitrary trade-off between the model accuracy and complexity: the channel segmentation method [26] and the spline-collocation technique [6, 11]. The latter is based on converting the partial differential equation expressing current continuity into a system of coupled ordinary differential equations (with the number equal to the number of collocation points) that can be readily solved by the circuit simulator. The use of the spline approximation for the charge density in the device is essential since the earlier polynomial approximations did not allow use of more than one collocation point. The details of this approach can be found in [6]. More recently this technique was extended to include all regions of operation in order to model transients involving the

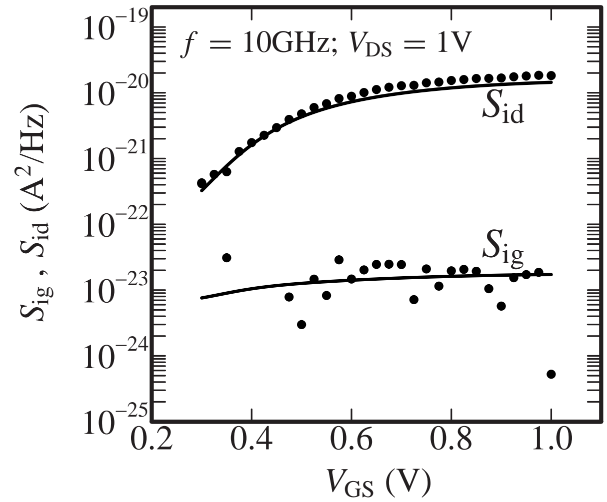

Figure 10: Drain (S_{id}) and gate (S_{ig}) current noise spectral density versus gate-source bias for an L=90nm n-channel device. Symbols denote measurements and lines represent modelled results using PSP

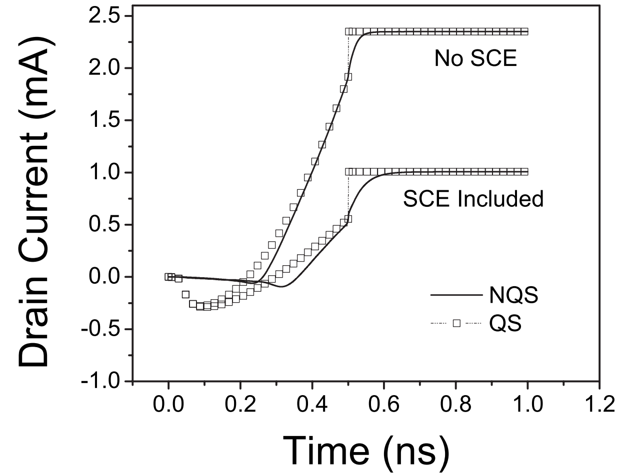

Figure 11: Transient response of 5/5μm MOSFET with and without short-channel effect (SCE). The gate voltage is ramped from 0 to 3V in 0.5ns.

accumulation region [11].

The NQS model developed for PSP includes modeling of short-channel effects. Typical results are shown in Fig. 11. The upper set of curves represents the case of constant mobility, while the lower set shows the simulation results when the mobility is degraded by the vertical field. In addition to the overall reduction of the current, mobility degradation lengthens the transients.

An important advantage of basing the NQS model on the solution of the continuity equation is that all terminal currents are automatically included and the large-signal and small-signal models are consistent with each other and with quasi-static simulations, which appear as a proper limiting case of slow transients or in the low-frequency limit. This is also true for the channel segmentation method.

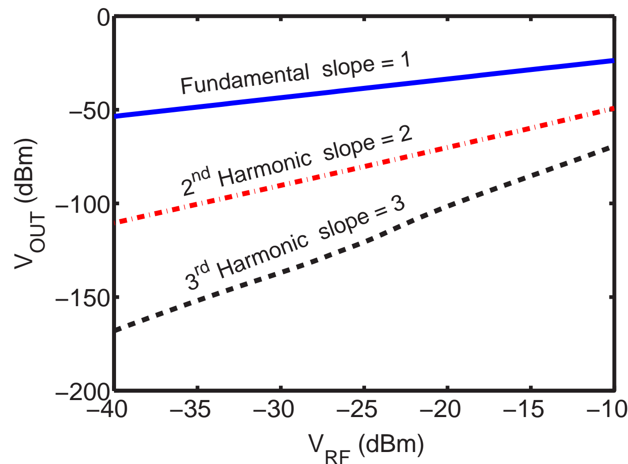

Figure 12: Intermodulation products for a simple RF CMOS mixer

10 SIMULATION EXAMPLE

As an example of circuit simulation using PSP we consider intermodulation (IM3) modeling of a simple passive mixer. Modeling of this circuit (that is of some interest to mobile communications) is a surprisingly difficult problem that has been solved only recently [14]. The issue is that (unlike the case for active mixers) passive mixer modeling is sensitive to any singularity at zero drain bias. The non-singular nature of PSP results in a correct slope (3 dB/dB) for the third harmonic (cf. Fig. 12). The circuit diagram and further details (some within the SP context) can be found in [14].

11 CONCLUSIONS

The commonality between SP and MM11 have been used to successfully merge both compact models into a powerful new model called PSP. This development required the expansion of the symmetric linearization method which has been shown to be sufficiently flexible for use outside of its original domain. The model has been subjected to the standard convergence tests and verified by comparison with data obtained from several 90nm and 60nm node processes. PSP satisfies all the requirements for a next generation compact MOSFET model.

Acknowledgments

PSP development at the PSU is supported in part by the Semiconductor Research Corporation, the Motorola Shared University Partnership Program and by the IBM University Partnership Award. The authors are grateful to C. McAndrew, J. Watson, P. Bendix, D. Foty, N. Arora, W. Grabinski, and S. Veeraraghavan for several illuminating discussions of the compact modeling methods, and to B. Mulvaney for the use of MICA simulator.

REFERENCES

[1] G. Gildenblat, H. Wang, T.-L. Chen, X. Gu and X. Cai, IEEE JSSC, 39, 1394 (2004)
[2] R. van Langevelde, A.J. Scholten and D.B.M. Klaassen, http://www.semiconductors.philips.com /acrobat/other/philipsmodels/mos-models/ model11/NLUR2002-802.pdf
[3] R. van Langevelde, A.J. Scholten and D.B.M. Klaassen, Proc. NSTI-Nanotech 2004, p. 60
[4] G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, Proc. ICECS 2004 (in press)
[5] T.-L. Chen and G. Gildenblat, Electron. Lett., 37, 791 (2001)
[6] H. Wang, T.-L. Chen and G. Gildenblat, IEEE TED, 50, 2262 (2003)
[7] H.C. Pao and C.T. Sah, SSE, 9, 927 (1966)
[8] J.R. Brews, SSE, 21, 345 (1978)
[9] Y. Tsividis, "The MOS Transistor", McGraw-Hill, 1999
[10] G.A.M. Hurkx, D.B.M. Klaassen and M.P.G. Knuvers, IEEE TED, 39, 331 (1992)
[11] H. Wang and G. Gildenblat, Proc. 2004 IEEE CICC p. 5
[12] C.-L. Huang and N. Arora, SSE, 37, 97 (1994)
[13] K. Joardar, K.K. Gullapalli, C.C. McAndrew, M.E. Burnham and A.Wild, IEEE TED, 45, 134 (1998)
[14] P. Bendix, P. Rakers, P. Wagh, L. Lemaitre, W. Grabinski, C.C McAndrew, X. Gu and G. Gildenblat, Proc. 2004 IEEE CICC p. 9
[15] R. van Langevelde, L.F. Tiemeijer, R.J. Havens, M.J. Knitel, R.F.M. Roes, P.H. Woerlee and D.B.M. Klaassen, IEDM 2004 Tech. Dig., p. 807
[16] T.N. Nguyen and J.D. Plummer, IEDM Tech. Dig., 1981, p. 596
[17] M. Miura-Mattausch, IEEE TCAD, 13, 610 (1994)
[18] T. Grotjohn and B. Hoefflinger, IEEE TED, 31, 109 (1984)
[19] N. Arora, R. Rios, C.-L. Huang and K. Raol, IEEE TED, 41, 988 (1994)
[20] D.E. Ward and R.W. Dutton, IEEE JSSC, 13, 703 (1978)
[21] D.B.M. Klaassen, R. van Langevelde and A.J. Scholten, IEICE Trans. Electron., p. 854 (2004)
[22] R. van Langevelde, A.J. Scholten, R. Duffy, F.N. Cubaynes, M.J. Knitel and D.B.M. Klaassen, IEDM 2001 Tech. Dig., p. 289
[23] X. Gu, T.-L. Chen, G. Gildenblat, G.O. Workman, S. Veeraraghavan, S. Shapira and K. Stiles, IEEE TED, 51, 127 (2004)
[24] R. van Langevelde, A.J. Scholten, R.J. Havens, L.F. Tiemeijer and D.B.M. Klaassen, Proc. ESSDERC 2001, p. 81
[25] G. Gildenblat, X. Cai, T.-L. Chen, X. Gu and H. Wang, IEDM 2003 Tech. Dig., p. 863
[26] K.K. Hung, P.K. Ko, C. Hu and Y.C. Cheng, IEEE TED, 37, 654 (1990)
[27] R. van Langevelde, J.C.J. Paasschens, A.J. Scholten, R.J. Havens, L.F. Tiemeijer and D.B.M. Klaassen, IEDM 2003 Tech. Dig., p. 867.