

How to Design for Analog Yield using Monte Carlo Mismatch SPICE Models

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ABSTRACT

In this paper, we propose a simple method to select minimum or maximum values for design parameters that will give us a desired analog circuit yield. Our method uses a 2-level Monte Carlo approach to predict yield as a function of the design parameter values. Using this approach it is easy to select the value of any design parameter such as gate length or width, to achieve a desired analog yield. We use Monte Carlo simulation of both mismatch and process variation in order to predict the yield of the analog circuit. By extrapolating from a small number of simulations we can save time. Then by plotting the results and working back we can determine the limit of the input design parameters that we should choose to achieve the desired analog yield.

Keywords: mismatch, analog, yield, Monte Carlo, SPICE, CMOS.

1 INTRODUCTION

Analog yield (or parametric yield) is defined as the percentage of chips or circuits that meet all analog output performance specifications [1,2]. During the design phase, analog circuit blocks are usually simulated over the full range of Process, Voltage, and Temperature (PVT) to make sure they will yield. However these PVT corner simulations cannot calculate the quantitative analog yield. This could lead to over-conservative designs or risky low yield designs. Of course the final manufacturing yield depends on additional factors such as defect density and can only be seen after the product is fabricated in production.

For digital designs two corners may be sufficient, the fastest and the slowest corner. For analog circuits however, the number of corner simulations required can be large. This PVT corner approach does not take into account mismatch of resistors, capacitors, BJTs, or MOSFETs for high precision circuits. PVT simulations do not provide a quantitative yield number. Analog circuit block yield needs to be very high to achieve good chip yield because the chip yield is the product of all the individual block yields. For example say a chip has 32 comparators. If the target chip yield is $Y = 99.56\%$ (i.e. 3-sigma), then each comparator block must yield $Y = 99.987\%$ (4-sigma). In this case, $Y_{chip} = (Y_{block})^N$.

We propose a simple way to predict analog circuit yield by using a 2-level Monte Carlo simulation with both

mismatch and process variation in the SPICE models. If only process variation were used, there would be no mismatch or offset voltage. If only mismatch models were used, then there would be no process variation. By using the Silterra 0.18um C18 MOS SPICE models with 2-level Monte Carlo, we can simulate both process and mismatch variation.

The simple CMOS differential amplifier circuit of Figure 1 will be used as an example. Although the circuit is almost trivial, it is easy to understand and the analysis method can be applied to much more complex circuits. The circuit has two poly resistors $R = 10K$ Ohm with $W/L = 1/33$ um/um and two NMOS transistors with $W/L = 10/0.18$. The voltage gain is about -16 when the gates are biased to 0.54V. VDD is 1.8V $\pm 10\%$. The offset voltage, VOS, is defined as the output when the input is zero. Offset is caused by mismatch of the two resistors and the two MOSFETs.

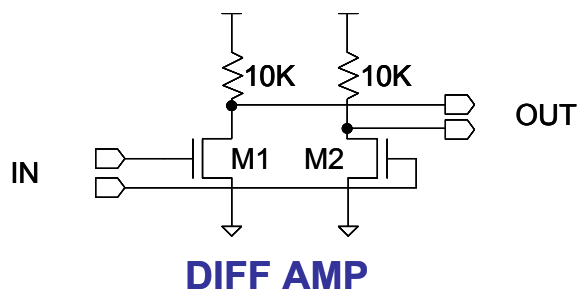


Figure 1: Simple CMOS differential amplifier example. The two NMOS transistors have $W/L = 10/0.18$ um/um.

2 P-V-T CORNER METHOD

Process corner SPICE models are normally supplied by the foundry or wafer fab. At Silterra, the models are designed so that they represent the full spec range of the factory's process variation. We take six BSIM model parameters to their extremes, (V_{th} , T_{ox} , D_L , D_w , R_{ds} , and C_j) while making sure the model outputs (I_D and V_T) exactly match the process electrical specifications.

For analog design, the number of possible corner simulations is $N = 2^M$, where M is the number of factors, each taking on min and max values. Figure 2 shows the concept of two process parameters and their effect on performance parameters. If Diffusion resistors, Poly resistors, Well resistors, MIM capacitors, BJTs, diodes,

Varactors, as well as MOSFETs each take on min and max values in addition to temperature and voltage, the number of simulations becomes unmanageable. Furthermore the PVT corner simulations alone do not simulate mismatch or calculate yield.

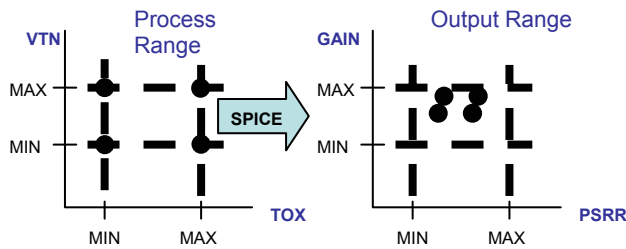


Figure 2: A conceptual example to illustrate the P-V-T (Process, Voltage, Temperature) Corner Method. Shown are two process parameters, threshold (VTN), and oxide gate oxide thickness (Tox), and two performance parameters, Voltage Gain (Av) and Power Supply Rejection Ratio (PSRR).

For example, four process corners (FF, SS, FS, SF), min and max temperatures, min and max VDD supply, and min and max poly resistors would require $4 \times 2 \times 2 \times 2 = 32$ SPICE runs.

3 SIMPLE MONTE CARLO METHOD

The Monte Carlo method randomly varies the inputs to represent the process variations. The distribution is usually assumed to be Gaussian. Figure 3 illustrates the concept. Two process parameters are shown, but any number of Monte Carlo parameters can be used. Typically $N = 30$ to $N = 50$ simulations are enough to get meaningful statistics. The number of runs is independent of the number of Monte Carlo variables.

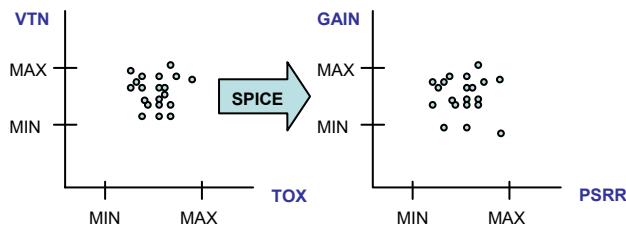


Figure 3: Conceptual example of the Monte Carlo Method showing random variation of two process parameters, threshold (VTN) and oxide gate oxide thickness, (Tox), and the effect on two performance parameters, Voltage Gain and Power Supply Rejection Ratio (PSRR).

Figure 4 shows the inputs VTN and TOX for 50 Monte Carlo simulations. We know there should be a slight correlation between VTN and TOX, but we let them vary independently. This makes the results slightly pessimistic.

The problem with simple Monte Carlo simulations is that the offset is still zero as in Figure 5. To simulate offset we need to run a 2-level Monte Carlo simulation described in the next section. We also have to simulate over the temperature and power supply range.

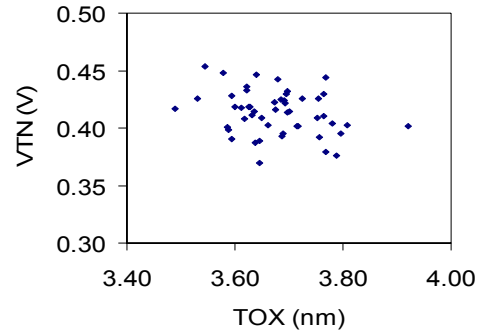


Figure 4: An example of the Monte Carlo Method showing random variations of two process parameters, threshold (VTN) and oxide gate oxide thickness (Tox).

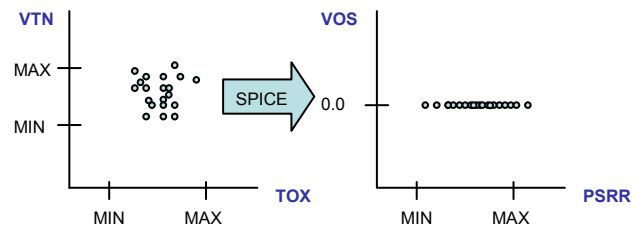


Figure 5: The Single-Level Monte Carlo simulations produce zero offset voltage (VOS) because all transistors and resistors in each pair are identical (no mismatch).

4 TWO-LEVEL MONTE CARLO METHOD

Mismatch can not be neglected. According to the inverse square root law [3], MOS mismatch becomes more severe when transistor gate area decreases. The downscaling of devices leads to larger V_t and I_d mismatch that can cause low or even zero analog circuit yield. Even in digital circuits, transistor mismatch is becoming one of the obstacles to achieving high yield. MOS V_t mismatch is shown in Figure 6. Figure 7 shows P+ Poly unsilicided resistor pair mismatch data.

The 2-level Monte Carlo method has two types of random variables. The first represents the lot-to-lot variation and the second represents within-die variation, or mismatch. Figure 8 and Figure 9 show both kinds of variable. VTN is different in each of the 50 simulations. On top of this each transistor in the circuit has random variation due to mismatch.

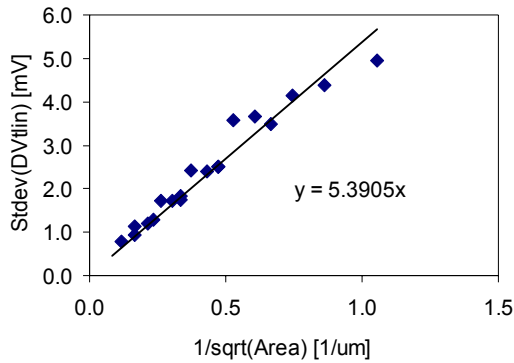


Figure 6: Measured NMOS V_t mismatch as a function of transistor gate area. The vertical axis is the standard deviation of the delta- V_t . Data is from 11 wafers, 32 sites per wafer. The 20 data points represent 20 NMOS pairs each having a different value of L and W. V_t is measured at $I_d = 0.1\mu A * W/L$ with $V_d = 0.1V$.

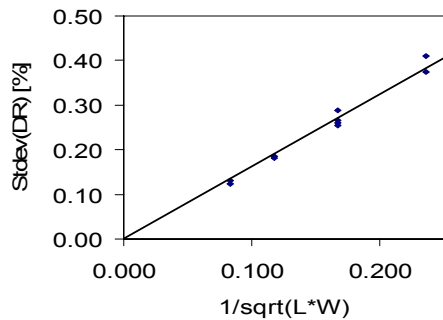


Figure 7: Measured P+ Poly resistor mismatch as a function of resistor area. The vertical axis is the standard deviation of the delta-R in percent. Each point represents the standard deviation of 345 resistor pairs. Ten different sizes of resistor were measured. Sheet resistance is 310 Ohm/sq.

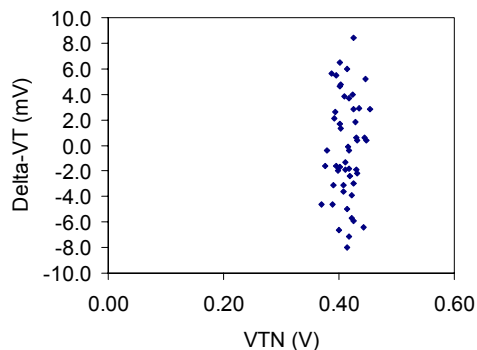


Figure 8: Example results of the 2-Level Monte Carlo Method showing both process variation (VTN) and intra-chip threshold mismatch (DVT), for $N = 50$. VTN and DVT are not correlated.

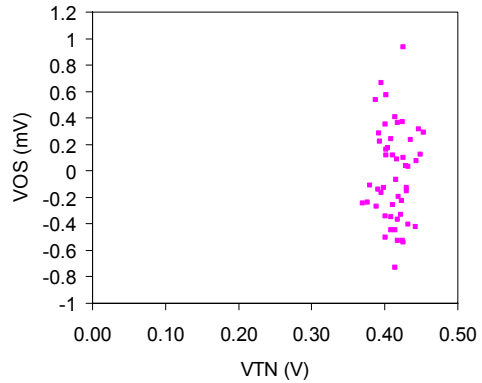


Figure 9: Example results of the 2-Level Monte Carlo Method showing performance (VOS) vs. process variation (VTN) for $N = 50$. VTN and VOS are not correlated.

5 YIELD CALCULATION

Figure 10 illustrates our method of predicting Analog Yield. We run 50 two-level Monte Carlo simulations, then plot the output as a “normal distribution” plot. The intersection of the extrapolated line with the VOS Spec is the predicted yield. This method requires only 30 to 50 Monte Carlo runs. This is much faster and more efficient than running 300 or 1000 simulations and counting the actual yield.

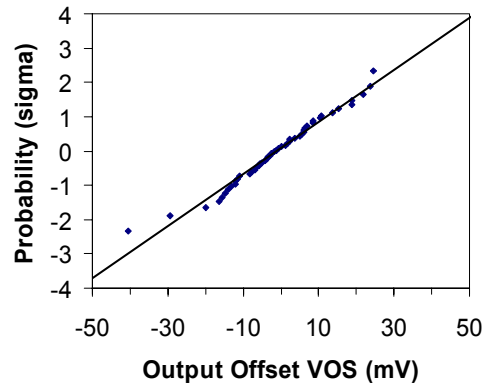


Figure 10: This is output offset (VOS) data from 50 Monte Carlo SPICE runs. The vertical axis is probability in “sigma” units. The line intersection with the VOS Spec is the predicted yield. If the offset spec is 40mV, the analog yield of this circuit will be about 3-sigma, or 99.56%.

6 HOW TO SELECT DEVICE SIZE

Now we wish to determine what is the required width and length of the NMOS transistor in the circuit of Figure 1. We need to keep the ratio W/L constant to fix the gain and operating point. First we set the desired yield goal, for

example $VOS < 40\text{mV}$, with block yield $Y = 99.56\%$ (i.e. 3-Sigma). Next we run four Monte Carlo experiments with different device width, W . Plot the output parameter (VOS) vs. W . Then select W to get desired VOS at the desired yield. In Figure 11, the width required is $50\ \mu\text{m}$ for 3-sigma yield. Note the resistor mismatch is included in the simulations, but we choose not to change the resistor size.

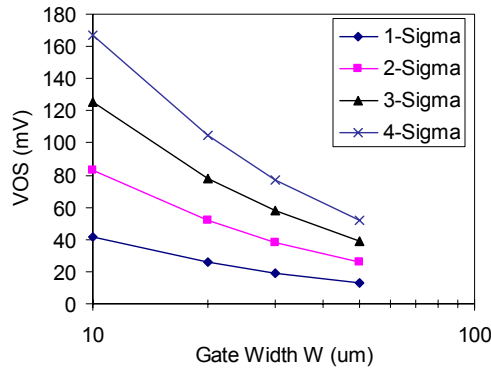


Figure 11: Plot of Offset Voltage (VOS) versus Differential Matched Pair Transistor Width. Four different yield targets are plotted.

7 CONCLUSION

The aim of this paper is to illustrate usage of mismatch models not only for analog yield prediction but for designing a circuit to achieve a given yield target. The 2-level Monte Carlo method shown in this paper will enable analog circuit designers to predict analog yield, and design achieve the desired yield goal.

Furthermore the method of calculating the device sizes necessary to attain a given yield will enable circuit designers to take into account the trade-off between matched device size and yield when designing their circuits. We hope this paper will give circuit designers more insight into their circuit's yield caused by transistor mismatch and process variation before going into fabrication.

8 ACKNOWLEDGEMENTS

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