## Carbon Nanotube-based Sensor Devices for IC Performance Evaluation

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### ABSTRACT

A novel approach to the problem of identifying failed integrated circuits on electronic circuit boards has been sought that would allow for drastically reducing the costs of the test equipment development and maintenance. This article describes our ongoing efforts toward developing the original concept of Molecular Test Equipment®. Our focus is on our progress in creating carbon nanotube-based sensors carrying out the integrated circuit performance monitoring functions in an integrated circuit substrate level, as well as on the problem of interfacing the molecular devices with the existing metallic circuitry of the integrated circuits. The two main areas of interest explored recently by our team in order to create the basis for such sensor fabrication were: (i) producing solutions of homogenously dispersed carbon nanotubes in organic solvents, and (ii) developing a method for controlling the process of nanotube deposition at specific location on the silicon substrate.

*Keywords*: carbon nanotube electronics, nanoscale sensors, IC failure detection

### 1 INTRODUCTION

Integrated circuit (IC) density is continuing to increase through advances being made in semiconductor physics, IC development tools, and other technologies that support the conception of smaller and more efficient devices. In addition, advances in electron-beam and other lithography techniques enable these increasingly smaller devices to be created on the substrate of an IC. Today's best and most precise lithography techniques can create devices with dimensions on the sub-micron scale. For example, in complementary metal-oxide-semiconductor (CMOS) devices copper/silicon dioxide (Cu/SiO2) interconnect structures exhibit a line width of 0.9 um (900 nm), with line spacing of 0.5 um (500 nm). The ratio of line width to line spacing in this case is approximately two to one.[1] Dimensions for aluminum/silicon dioxide (Al/SiO2) interconnect structures exceed those of copper. Hu and Harper have documented the superior performance of Cu over Al through improved conductivity and reduced electromigration properties.[2] Based in part upon these trends, we anticipate that copper interconnects are likely to replace aluminum in future IC designs. Utilizing the newest developments in lithographic techniques, dimensions are expected to continue to decrease to the 100 nm range (close to the predicted limitation of conventional IC manufacturing capabilities) in the 2005 time frame.[3]

With nanotube device dimensions ranging as small as five to 30 nanometers, we are attempting to take advantage of the "empty space" that exists between and among conventional IC designs to provide internal IC testing capability without interfering with existing chip functionality.

Our approach involves the use of nanotube-based sensors as part of an overall Molecular Test Equipment (MTE) architecture to monitor the internal chemical composition of ICs and to measure electrical signal activity to determine their operational status. Traditional test methodologies have typically employed a "black box" approach whereby the IC is poked and prodded from the outside (stimulus is applied) to see its reaction (response signals are analyzed). If the reaction is generally what we expected to see, we then assume the IC is operational. This approach only approximates a complete test, and cannot tell whether problems internal to the IC exist that may be indicative of imminent failure or degraded performance now or in the future. The present process we have described requires a large investment in test equipment, interface devices, and software.



Figure 1: MTE-augmented Integrated Circuit

The presence of nanotube-based sensors within the IC provides us with access to structures where we can measure chemical and electrical signal activity from the inside – where the actual circuit operations are taking place. This

gives us the added advantage of measuring test points directly where failures are most likely to exist, and requires no investment in expensive external hardware and software to determine the outcome of testing. For manufacturing purposes, we anticipate the carbon nanotube-based sensors will be formed in a catalytically- and electrically-controlled self-assembly process; therefore, the cost for incorporating the MTE components within the ICs themselves is expected to be negligible comparing to the overall cost of the IC chip production. It is our intention that the cost increase will range from fractions of a penny to a few cents per chip, depending on quantity.

Sensor signals are communicated to a surface-mounted display device on the IC through the use of a combination of conventional and molecular wires, as well as conductive nanotubes in highly "crowded" locations. We describe our efforts for growing nanotubes using electrode material consisting of existing IC signal paths as a catalyst and address the specification of the conditions at which the properties of the created nanotubes meet the test requirements. These properties include the length of the nanotubes as well as their electrical properties (i.e., semiconducting or metallic).

## 2 MTE ARCHITECTURE

The nanotube-based chemical and electrical sensors comprise a fundamental portion of the overall MTE architecture. Additional components of this architecture include a surface-mounted failure indicator and one or more communication conduits through which sensor signals are sent to the failure indicator.

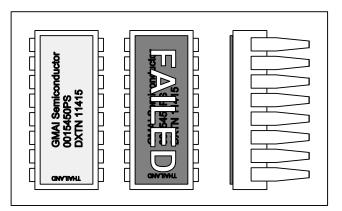


Figure 2: Molecular Test Equipment Schematic

A carbon nanotube, with an appropriate chiral structure allowing it to act as a metal wire, will conduct an electrical signal from the nanotube-based sensor to the surface mounted failure indicator. The input to the nanotube is a signal from the sensor. We are currently attempting to perform a comprehensive study to determine the range of voltages that a single nanotube may conduct. We are also considering the use of conventional micro-wires as a

supplement to carbon nanotubes as a communication conduit.

The failure indicator provides a visual indication to a technician as to whether the IC is good or faulty. This indicator is designed for mounting upon the surface of the chip to ensure adequate visibility. A key requirement of this indicator is that there be minimal impact to the form, fit, and function of the chip. For example, we anticipate low power requirements with a small footprint on the surface of the chip with little increase in chip height. Fault indicator fabrication is being accomplished to produce a simple TN-LCD device with the undemanding requirement that it has a low driving voltage. We anticipate a maximum driving voltage limit of 2.5 V, and a current requirement in the microampere regime for a 0.5 cm x 0.5 cm LCD device.

Translation of these architectural features into practice where ICs that can fully test themselves and notify a technician of a failure through a visual indicator is pictured in the Figure 1 showing a photograph of our MTE demonstration model. In the event of failure, an electrical signal is transmitted to the fault indicator. The indicator is expected to be extremely thin and not require any significant increase in IC height what is illustrated schematically in Figure 2.

### 3 RESEARCH PROGRESS



Figure 3: CNT-based metal migration sensor

One of the first types of sensors being targeted for the demonstration of our failure analysis system are metal migration sensors intended to detect IC failures coming from electromigration, hillock growth on metal conductors or electronic components, as well as the melting of some low melting-point metals. Carbon nanotubes have shown many specific properties, one of them is the high conductivity. Based upon their small size, one-dimensional molecular wires can be fabricated. When this carbon nanotube wire is placed on the empty area between signal paths within ICs, if electromigration of signal path materials or melting of signal paths occurs, a change in conductivity of the nanotube will occur and the event can be detected. This configuration is illustrated in Figure 3.

Essential to using carbon nanotubes as functional elements in electronic test equipment their processability allowing for achieving our desired configuration, and also their ability to perform electrical tests on the engendered nanoscale structures. We currently are assessing:

- techniques that will result in the assembly of molecular wires and carbon nanotubes into desired architectures on desired substrates, in readiness for their connection to metal electrodes,
- techniques that will result in the creation of robust contacts and connections between the molecular wires, carbon nanotubes, and the metal electrodes that they eventually will be connected to, and
- the possibility of using a combination of scanning tunneling microscopy (STM) and conductive probe atomic force microscopy (CP-AFM) to evaluate the nature of the nanostructured electronic ensembles required for the development of our nanosensor-pin testing paradigm.

Our efforts to date have primarily targeted the areas related to the development of suitable solvent systems able to produce homogenously dispersed suspensions of carbon nanotubes and the issue of controlled deposition of carbon nanotubes on desired substrates. Our findings related to this matter are presented in the paragraphs that follow.

# 3.1 Homogenous Dispersion Of Carbon Nanotubes

Well-dispersed carbon nanotube (CNT) solutions are a basis for not only the correctly performed deposition process but for a whole spectrum of procedures, including carbon nanotube purification, CNT functionalization, creating CNT-based composites, and many others. Developing a methodology for untangling the nanotuberopes and dispersing CTNs into a uniform solution would create a major impact in the entire field of nanotechnology. We tested our original idea of surfactant-assisted dispersion of CNTs in organic and inorganic solvents. Although the procedure we used still requires optimization, we managed to prepare nanotube solutions with dispersion rates far better than those obtained in the commonly used processes as shown in Figure 4.

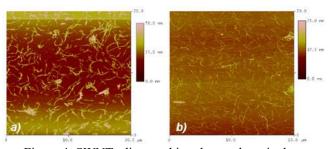


Figure 4: SWNTs dispersed in toluene, deposited on Si/SiO2/APTS wafer.

By using surfactant-based solvent systems, we have successfully untied a great portion of the single walled carbon nanotube (SWNT) ropes and evenly distributed them within the solution. We have also presented a method of controlling the deposition of SWNTs on the silicon substrate by tuning the concentration of the SWNT solution. Non-polar solvents, specifically toluene and N-Methyl-2-pyrrolidinone (NMP), presented the best results out of the group tested. At this point it is unclear what was the exact mechanism of the improved dispersion caused by the surfactant addition, however, it is expected that it was one of the following two processes: (1) the long aliphatic chain of the surfactant was wrapping around the nanotubes "pulling" them out of the bundle, or (2) the interactions between the aligned surfactant's aromatic rings and the nanotubes form structures, where the aliphatic chains are left sticking out preventing the nanotubes from re-tangling together.

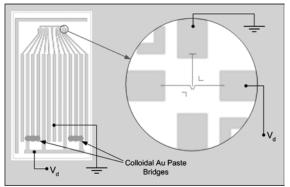


Figure 5: SWNT deposition on a test bed. Deposition potential  $V_d = 10V$  peak-peak AC (5MHz)

# 3.2 Nanotubes Deposition and CNT-wire Contacts Formation

Collaborative activities between GMA Industries, Inc. and NASA Langley Research Center have also resulted in well-developed competences to deposit, align, and subsequently connect carbon nanotubes with metal and metallized electrodes, through a process known as AC electrophoresis [4],[5].

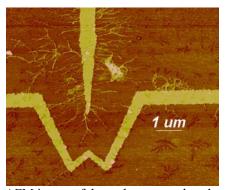


Figure 6: AFM image of the carbon nanotubes deposited at the central area of our W-shaped gold test bed circuit on Si/SiO2 wafer.

In our experimental method, nanotubes homogeneously dispersed in our developed solvent system were deposited onto a test bed fabricated for this purpose. One electrode of the bed was thereafter grounded and a potential was applied to the other electrode to create an electric field between the electrodes (as depicted in Figure 5). Upon the application of a potential, robust connection between the nanotubes and the metal electrodes was realized. AFM micrographs revealed that these nanotubes were well aligned and in concert with applied electric field lines (Figure 6). Measurements showed that the resistance through the test areas was 35 k $\Omega$ , which proved the robust connection formation: these connections maintained their rigidity even after being blown with nitrogen. It is clearly evident that the localization of the nanotubes can be controlled to great extent using the electric field alignment method. This concept will assist efforts to fabricate nanotube-based circuitry and specifically the MTE sensors including the metal migration sensors.

#### 4 CONCLUSIONS

Annual non-recurring costs for the development of automatic test equipment and test program sets and the recurring costs for their operation and maintenance runs into the billions of dollars. Our approach has a potential to significantly reduce costs associated with maintenance of circuit boards by embedding MTE embedded within ICs to enable them to continuously test themselves during normal operation, and to provide a visual indication that they have failed. This approach brings failure detection down to the atomic level, where we will be able to recognize changes in the structure of the material itself.

Future work will build upon this success through the development of prototype demonstration technology that will form the basis for use in IC production. It is likely that future nanoscale ICs will be extremely fast, small and energy efficient, and low cost devices that can be embedded within new IC designs as they evolve. Further, this technology can be adapted to provide a wide range of additional information regarding device operation, such as hours of operation, device temperature, etc. Our MTE concept is anticipated to be capable of being retrofitted into existing IC designs with minimal impact on IC functionality or change to current fabrication methods. As IC technology continues to shrink into the nanometer realm, MTE will be fully capable of being integrated directly into these new IC designs.

#### **ACKNOWLEDGMENTS**

We gratefully acknowledge the participation of Buzz Wincheski and the Nondestructive Evaluation (NDE) Research Group at NASA LaRC in the experimental portion of the research presented in this paper.

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