Silicon Nanostructures Patterned on SOI by AFM Lithography

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ABSTRACT

The actual trends in microelectronics are the reduction of the dimensions and the search of new devices standing upon new phenomena as in the case of a Single Electron Transistor (SET) that is based on the Coulomb blockade. The nowadays limitation for device dimensions is that we are reaching the resolution limits of the lithography techniques. To go beyond this problem, we use the Atomic Force Microscope (AFM) nanolithography. To all the advantages brought by this technique we add those of using a silicon-on-insulator (SOI) substrate. In this article we are showing an example of a nanostructure fabricated by this method. Transport measurements and simulations performed on the device are in good agreement.

We demonstrate the potential of using AFM lithography fabricated devices for applications like multi-gate transistors.

Keywords: AFM lithography, SOI, single electron devices

1 INTRODUCTION

Scanning probe microscopy (SPM) is a reliable technique that allows imaging and modification of the surface structure of the materials down to nanometric scales. The main advantage of SPM tools is the use of near-field interactions that allow a precise positioning of the probe (tip) next to the surface of the sample, which implies atomic resolution in the vertical plane. Other advantages of AFM techniques are its compatibility with the actual CMOS technologies and the fact that there are no proximity effects like in the e-beam technique.

The probe can induce different kind of changes in the surface, for example the local oxidation of the surface of the sample by application of a voltage on the tip. The feasibility demonstration was made in 1990 by using another SPM technique, the Scanning Tunneling Microscopy (STM) oxidation on a Silicon surface [1]. Different ways of improving the technique were proposed : oxidation in tapping mode [2], the use of a pulsed tension on the tip [3]. We have chosen to use the oxidation by AFM in contact mode.

Another advantage of our technique is the use of silicon-on-insulator (SOI) substrates. They ensure very thin monocrystalline top Si films with high quality interfaces, that are very important if we want to validate a reproducible process to fabricate the nanostructures.

Using the AFM induced local oxidation on a SOI substrate, we have obtained silicon nanowires with lateral gates.

2 FABRICATION PROCESS

The principle of AFM lithography on SOI was described for the first time by Campbell et al. [4]. Later results by this technique are presented in the references [5], [6].

The first step is the passivation of the Si wafer during a HF (2%) treatment. This allows the saturation of the silicon surface in Si-H. The hydrogen atoms can be locally replaced by oxygen under the influence of a negatively biased tip, as shown in Figure 1. It is similar to an electrochemical anodization. The only precaution is that the tip voltage must be more negative than the threshold voltage (-2.7V) [7], [8].

As the process appears only if there is a thin layer of water at the surface of the sample, the humidity must be kept constant and about 30%-40%. The speed of the tip while drawing the oxide line is 0.1µm/s. With these parameters we have obtained oxide patterns of 0.5-1.5nm high and about 50-70nm wide [9].

In figure 2 we are showing an example of a nanowire with lateral gates obtained by this technique.

The oxide patterns can be used as a mask during the silicon etching process. We are using a wet etching technique, by tetramethyl-amino-hydroxide (TMAH), that ensures a very high selectivity Si/SiO_2 (2000:1) [10].

The substrates used are Unibond ® silicon-on-insulator [11] samples with an ultra-thinned monocristalline Si layer down to 15nm and with a 400nm buried oxide thickness. The samples are doped by Arsenic ion implantation at 8keV, with two different surface doses : $5x10^{11}cm^{-2}$ and $2x10^{13}cm^{-2}$. This means that we can perform electrical measurements on samples of two doping levels, $2x10^{17}cm^{-3}$ and $10^{19}cm^{-3}$.

Conductive pads are already present on the samples. They are doped by Phosphorus and their doping level is about $2.5x10^{20}cm^{-3}$.

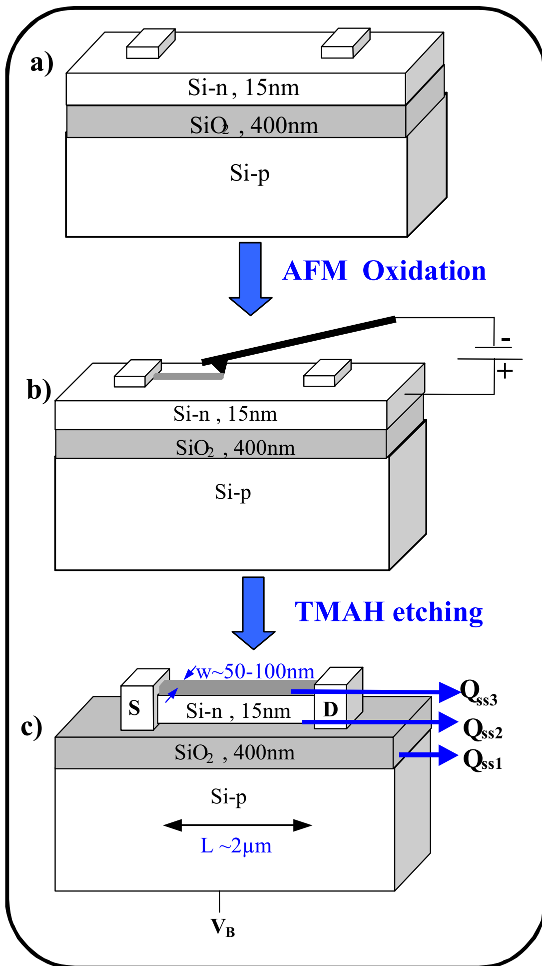

Figure 1 : Principle of AFM nanolithography: a) initial substrate, b) AFM oxidation, c) final structure after TMAH etching. In c), Q_{SS} represents the charge levels at each Si/SiO_2 interface.

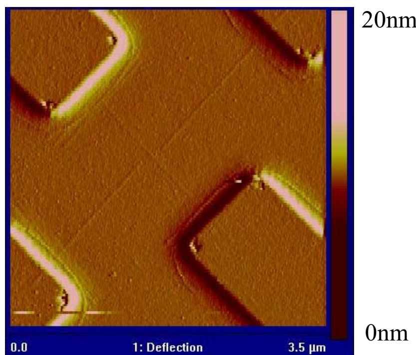

Figure 2 : SiO_2 nanowire designed by AFM lithography. In this example the wire is about 2.5µm length, 50nm width and 1nm high.

3 BACKAGATE EFFECT ON I-V CURVES

The first electrical tests were done on a nanowire of 2.5µm length, 15nm height, 100nm width and $2x10^{17}cm^{-3}$ doping level. The influence of the backgate voltage, V_B, on the I-V characteristics is shown in Figure 3.

We are observing the same kind of behavior as in a MOS transistor, normally on. For a negative bias on the backgate, the wire is in depletion and the resistance is decreasing as a space charge region appears and is increasing. For a positive bias, the wire is in accumulation.

On this wire, measurements were performed for biases down to –50V on the backgate; the wire was still conducting even if it should be completely deserted for V_B smaller then –3V. One hypothesis is that there is a native oxide layer that is formed on the surface and the interface between this oxide and the thin silicon layer does not have a very high quality. In this case, the conduction through the wire seems to be ensured by the charges located at the interface.

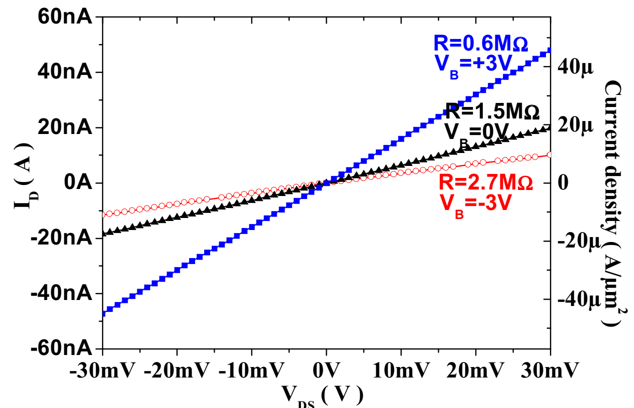

Figure 3 : Influence of the backgate voltage, V_B, on the I-V characteristics. The transistor-like behavior is evidenced.

4 ELECTRICAL SIMULATIONS FOR BACKGATE EFFECT

Simulations were performed using Silvaco simulator [12]. The structure simulated has the same geometrical and physical properties as the one used for electrical measurements (Figure 4). The influence of the backgate bias is the same as in the measurements for positive values. For negative values, the current through the nano-wire is zero. In this example, the interface charges have not been considered.

In Figure 5, we have introduced in our simulation interface charges at all the Si/SiO_2 interfaces (as shown in the Figure 1c). We can observe that the current for negative backgate biases is no longer zero, but the values of the resistance are changing quite a lot from those measured during the electrical characterization.

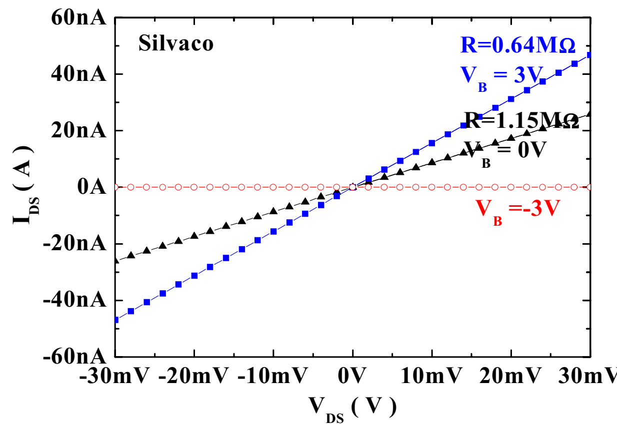

Figure 4 : Silvaco simulations without considering interface charges.

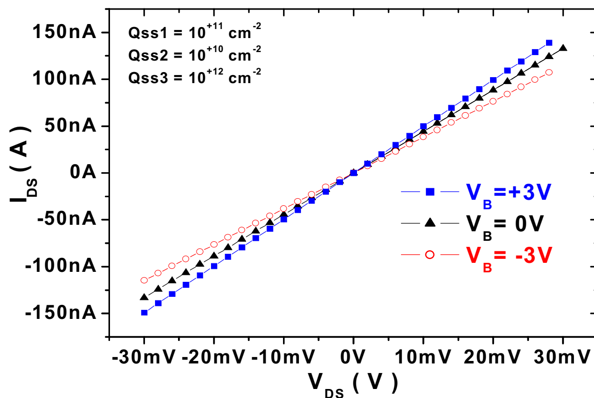

Figure 5 : Simulations considering interface charges. The position of the various Q_{SS} is shown in the Figure 1c.

5 SURFACE TREATMENTS

The fact that the interface charges seem to have such an importance on the conduction in the wire gave us the idea of trying to investigate the effect of surface treatments on SOI. We have tested the effect of a rapid thermal annealing (RTA) on the conduction through a SOI thin layer.

During the cleaved step we create defects in the structure of the thin layer of silicon and this induces an increase of the resistance value. If we add a rapid thermal annealing step, we are able to improve the qualities of this layer, so the resistance decreases (Table1).

Treatment	Resistance
SOI	65Ω
Cleaved SOI	106Ω
RTA SOI	82Ω

Table 1: Evolution of the resistance at different fabrication stages.

6 LATERAL GATES EFFECT ON I-V CURVES

The tests were done on a wire with two lateral gates having the same type of geometry as the first one, but with a doping level of $10^{+19}cm^{-3}$. Figure 6 shows the effect of the lateral gates bias on the conduction through the wire. The measurement was done without applying any voltage on the substrate. The shape of the I-V is the same as for a classical TMOS transistor.

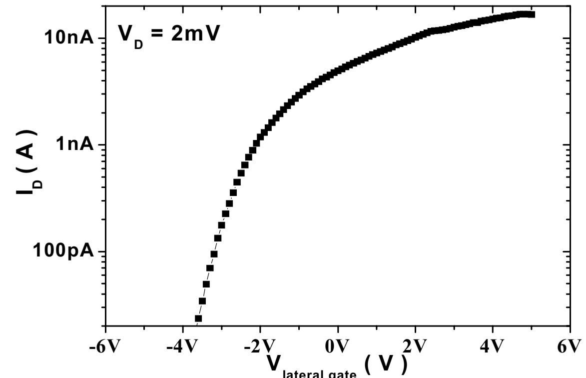

Figure 6 : Influence of the lateral gate voltage on the I-V characteristics

7 CONCLUSION

We have shown the feasibility of fabricating nanostructures on SOI substrate by using an AFM nanolithography technique. This tool is very promising for future applications because it is completely compatible with the actual CMOS technology, since we operate on SOI substrates, and it has the resolution required for the nanotechnology devices. The electrical characterization showed the influence of the backgate bias on the conduction in the wire. The same kind of behavior is observed for the lateral gates bias. So we have demonstrated the functioning of these nanostructures as multi-gates transistors.

Simulations had shown that the interface charges have a large impact on the conduction in the wire. Surface treatments like rapid thermal annealing (RTA) can improve the characteristics of the material.

In perspective, we shall make measurements of the electrical transport, especially at low temperatures, in order to study monoelectronic effects like Coulomb blockade. Comparisons between different architectures and different doping levels are going to be done. The impact of different surface treatments on the conduction will be studied.

The objectives of our work are to design nanostructures that can be used in applications based on monoelectronic devices: Single Electron Memory or Single Electron Transistor...

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