A Study of the Threshold Voltage Variations for Ultrathin Body Double Gate SOI MOSFETs

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ABSTRACT

Silicon on insulator (SOI) devices have been of great interest in these years. In this paper, simulation with density-gradient transport model is performed to examine the variation of threshold voltage (V_{TH}) for double gate SOI MOSFETs. Different thickness of silicon (Si) film, oxide thickness, channel length and doping concentration are considered in this work. According to the numerical study, both drift-diffusion (DD) and density gradient (DG) models demonstrate that the thickness of Si film greatly affects the threshold voltage (5 ~ 15 % variation). It is found that the thickness of Si film decreases, V_{TH} variation increases; and the dependence relation is nonlinear. Therefore, this effect must be taken into account for the realization of double gate SOI ULSI circuit.

Keywords: double-gate devices, ultrathin body, quantum mechanical effects, threshold voltage, modeling and simulation.

1 INTRODUCTION

Double gate SOI devices are more and more attractive for sub-50 nm ultra-large scaled integrated (ULSI) circuits manufacturing because of their inherent suppression of short-channel effects (SCEs), high transconductance and ideal subthreshold swing (S-swing) [1-9]. The double gate SOI devices, owing to a difficulty of manufacturing uniformity, suffer fluctuations of silicon and gate oxide thin films. This is important for design and fabrication of the double gate SOI devices, in particular for the applications of ULSI circuits. From the fabrication point of view, the double gate SOI manufacturing may have a 10 % thin film thickness fluctuation. Therefore, threshold voltage variation resulting from this fluctuation becomes an important problem and should be subject to further investigation when exploring important information for circuit designer and device engineer. Besides the thickness discrepancy in Si thin film, the correlations between the gate oxide thickness variations to threshold voltage changes should also be examined. Considering these two non-uniformity properties for the double gate SOI device, we probably can ensure the ability for double gate SOI ULSI circuit design and manufacturing. Various works have recently been proposed for these devices [1-16].

In this work, we computational examine the fluctuation effects of Si film thickness on the threshold voltage variation. In the numerical simulation of the threshold voltage variation, the classical and quantum correction transport models, DD and DG models are considered and solved numerically [10-14]. Addition to the thickness variation effects, the doping concentration, oxide thickness, and channel length are simulated systemically to discuss the threshold voltage variation. Subjecting to the comprehensive numerical studies, the complete conclusion and suggestion are drawn.

2 COMPUTATIONAL MODELS

Classical and quantum models are employed to compare the quantum effects on the threshold voltage variation. DD and DG models are considered in this work. Firstly, the three governing equations of DD model are listed in the following. Equation (1) shows the Poisson equation:

$$\nabla \varepsilon \cdot \nabla \psi = -q\left(p - n + N_D - N_A\right), \tag{1}$$

where ε is the electrical permittivity, q is the elementary electronic charge, n and p are the electron and hole densities, and N_D and N_A are the number of ionized donors and acceptors, respectively. The other two are continuity equations, they are presented in the equations (2) and (3), respectively:

$$q\frac{\partial n}{\partial t} - \nabla \cdot \mathbf{J_n} = -qR, \tag{2}$$

$$q\frac{\partial p}{\partial t} + \nabla \cdot \mathbf{J_p} = -qR, \tag{3}$$

$\mathbf{J}_n$ and $\mathbf{J}_p$ are the electron and hole current densities while μ_n and μ_p are the electron and hole mobility. Moreover, it should be noticed that ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials.

It is known that in comparing with the classical simulation, the quantum mechanical model explores different deviation quantitatively. In principle, the Schrödinger equation coupled with classical model is the most accurate way to solve the carrier concentration. However, it is not only computationally expensive but also difficult in simulation of multi-dimensional cases. Consequently, researchers devote their efforts on developing of quantum correction models. Those models are claimed to have a similar result as quantum mechanically calculated one but requires the same computation cost as that of the classical calculation. To include quantization effects in a classical device simulation, a simple approach is to introduce an additional potential, such as quantity Λ, in the classical density formula, which reads:

$$n = N_C \exp\left(\frac{E_F - E_C - \Lambda}{k_B T}\right), \quad (4)$$

where N_C is the conduction band density of states, E_C is the conduction band energy, and E_F is the electron Fermi energy. It is difficult to describe all quantum mechanical effects in terms of a variable Λ. A carefully quantum correction should be taken into considerations for avoiding any under- or over-estimations. Among the quantum correction models, DG model is a well-known approximation [15]. We chose it in this work and Λ is:

$$\Lambda = -\frac{\gamma \hbar^2}{12m} \frac{\nabla^2 \sqrt{n}}{\sqrt{n}}, \quad (5)$$

where $\hbar$ is the reduced Planck constant, m is the density of states mass, and γ is a fitting factor.

The computing procedure is briefly described as follows. Firstly, the stop criteria, mesh, output variables and simulation models are chosen. If DD model is chosen, Poisson equation is solved iteratively until the result converges. If DG model is chosen, the modified potential should be added in Poisson equation and solved. Then, continuity equations are solved. After all equations converge, we check the convergence of whole system. If the whole system converges, the simulation is terminated. Otherwise, we perform the outer loop iteration until it converges. This scheme produces a self-consistent result.

3 RESULTS AND DISCUSSION

In our numerical studies, the influence of oxide thickness (T_{OX} = 1.5, 2, 3 and 4 nm), channel length (L_G = 35, 65, 90 and 130 nm), Si film thickness (T_{Si} = 20, 40 and 65 nm) and doping concentration (N_A = 1×10^{17}, 5×10^{17}, 1×10^{18}, and 5×10^{18} cm^{-3}) on the threshold voltage for double gate SOI n-typed MOSFETs is simulated using ISE-DESSIS ver. 8.0.3 [17]. Each factor is examined sequentially. The definition of threshold voltage employed in this study is the Gm maximum method. The method firstly find out the gate voltage at the maximum of Gm, then make a tangent line of the drain current – gate voltage (I_{DS}-V_{GS}) curve at the gate voltage. Finally, extrapolated intercept of the tangent line to the V_{GS}-axis; the extrapolation is defined as V_{TH}.

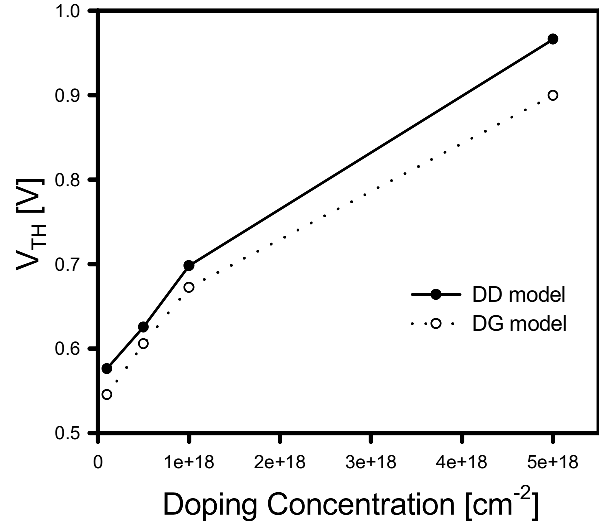

Figure 1: V_{TH} vs. the doping concentration. They are computed with DD (solid line) and DG (dot line) models.

The influence of doping concentration on V_{TH} is discussed firstly. Different doping concentrations of a 65 nm double gate SOI NMOSFET with T_{OX} = 1.5 nm and T_{si} = 40 nm are simulated with DD and DG models, shown in Fig. 1. It is found that V_{TH} increases as doping concentration increases. Therefore, a heavy doped substrate reduces V_{TH} roll-off caused by SCE. The variation is almost linear. An increase of 10^{18} cm^{-3} in doping concentration induces a 0.13 V shift on V_{TH}. From Fig. 1, the V_{TH} variations of the heavy doping devices are smaller than that of light doping ones. In comparing the extreme cases of the scenario, we observe a 30 % variation of V_{TH}.

Next, the threshold voltage affected by Si film thickness is discussed. A 65 nm double gate SOI NMOSFET with T_{OX} = 1.5 nm and N_A = 5×10^{17} cm^{-3} is explored and presented in Fig. 2. Both DD and DG models demonstrate that the thicknesses of the Si film will greatly affect the threshold voltage of the double gate devices. We note that the decrease of T_{Si} results in a significant increase on V_{TH}. For example, a 10-nm-thin T_{Si} shifts V_{TH} up to 0.02 V (~ 4% variation). This phenomenon is mainly caused from the shield-effect that retards the SCE. Thus, employing a thin Si film of double gate SOI NMOSFET will enhance the scaling down ability of semiconductor devices. From the fabrication point of view, the manufacturing may have a 10 % fluctuation in thin film thickness; accordingly, a 0.01 V variation of V_{TH} should be carefully estimated for manufactured devices.

Oxide thickness scaling effects is shown in the following paragraph. Figure 3 exhibits the simulated results of a 65 nm double gate SOI NMOSFET. T_{Si} and N_A are 40 nm and 5×10^{17} cm^{-3}, respectively. Since the gate oxide thickness scaling results in an oxide capacitance increases. Additionally, V_{TH} decreases when the oxide capacitance increases. This implies that the change of V_{TH} is linearly dependent on T_{OX}. From our simulation results, a nanometer decrement of T_{OX} will cause a 0.014 V (~ 2.2 %) threshold voltage decrement. The extreme cases of the simulated scenario are about 7 % variation of V_{TH}.

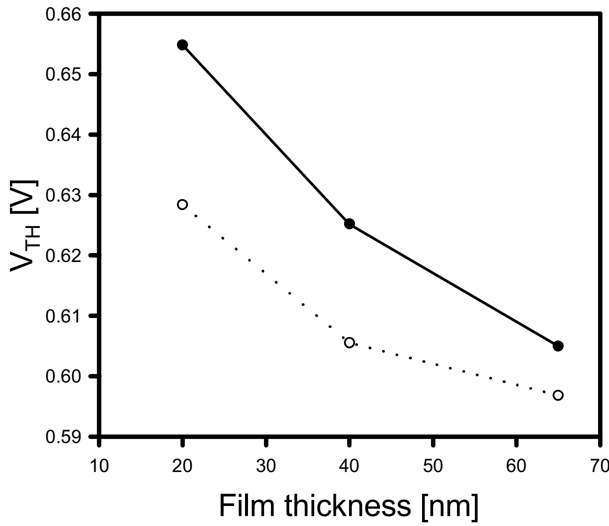

Figure 2: V_{TH} vs. T_{Si} . The notations are the same with Fig. 1.

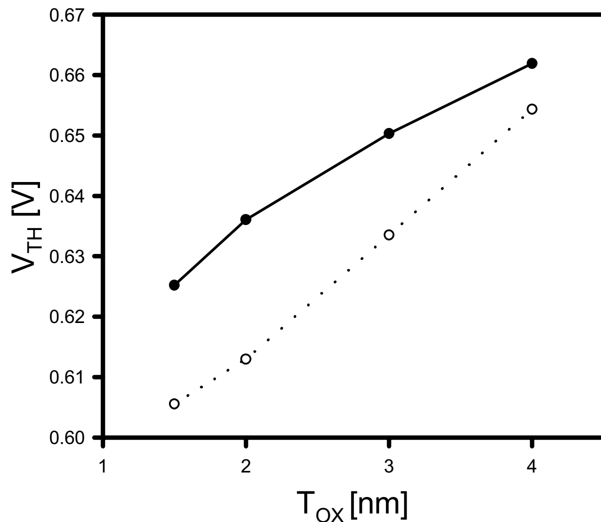

Figure 3: V_{TH} vs. T_{OX} . The notations are the same with Fig. 1.

Figure 4 plots the double gate SOI NMOSFET simulated results of V_{TH} vs. the channel length. T_{Si} = 40 nm, T_{OX} = 1.5 nm, and N_A = 5×10^{17} cm^{-3} are chosen in this examination. We observe that the shield-effect strongly reduces drain-induced barrier lowering (DIBL) that roll-off of V_{TH} does not so sensitive to channel length scaling. Take a realistic number for example; a 10 nm reduction on the channel length induces 0.04 V (~7 %) decreasing of V_{TH}. Furthermore, Fig. 4 suggests that the threshold voltage lowering effects would become serious when the channel length scaled down.

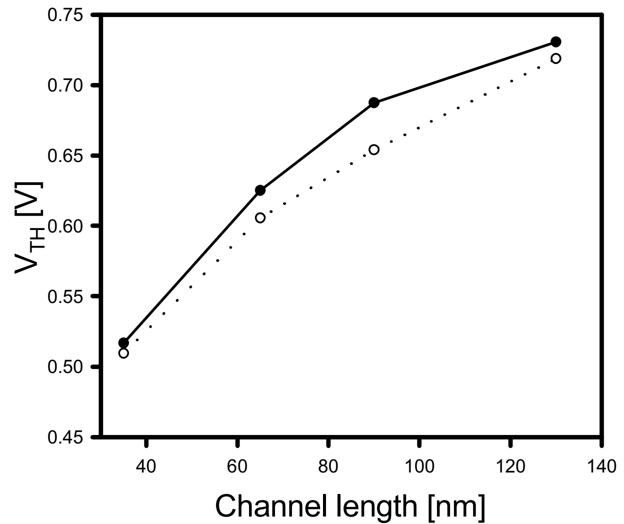

Figure 4: Simulated curves of V_{TH} vs. the channel length for DD and DG models.

In summary, from Figs. 1 to 4, the quantum effect on the V_{TH} variation is explored. According to these figures, DD and DG models predict similar V_{TH} variation under different device characteristics. However, DD model overestimates V_{TH} for about 4 %, which is about 0.03 ~ 0.05 V. Those facts are strongly related to electron distributions difference between classical and quantum theories. Therefore the quantum effect should be included in nanoscale semiconductor devices simulations.

To clarify the fluctuation of Si film thickness related V_{TH} variation, the DG simulation is performed for different film thicknesses and doping concentrations. Those results are shown in Fig. 5 that higher V_{TH} variation will be concluded for a thinner film thickness (~ 5 % for T_{si} = 20 nm); moreover the variation is nonlinear dependency. Therefore, this effect must be taken into account for the thinner silicon film double gate SOI ULSI circuit.

From the standpoint of devices physics, problems should be overcome are SCE and nonscalability of the oxide thickness scaled down to about 1.5 nm. The practical limit does not allow us to scale down devices feature and keep a constant ratio between channel lengths to oxide thickness. The shield-effect of double gate SOI NMOSFET minimizes the short channel effects and makes drain current improvement with device scalability enhancement. In addition, a manufacturing error exists during the devices fabrication. According to the results, V_{TH} depends on T_{Si},

T_{OX}, N_A and L_G. The relationship among them can be expressed as nonlinear function (6)

$$V_{TH} = f(N_A, -T_{Si}, T_{OX}, L_G), \quad (6)$$

where f should be subject to further formulation. As mentioned above, V_{TH} fluctuates severely in the extreme small devices. Therefore, all effect should be considered in the fabrication of nanoscale double gate SOI NMOSFETs.

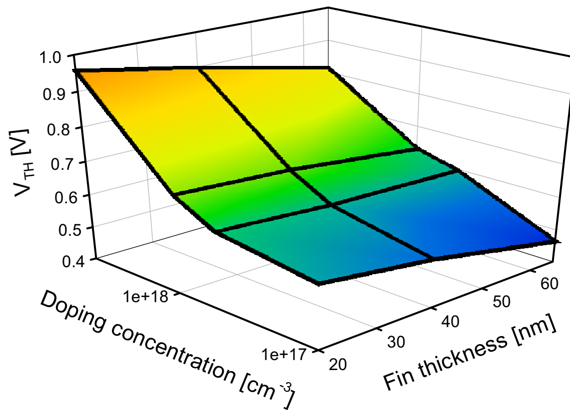

Figure 5: A three-dimensional plot of V_{TH} with respect to the doping levels and film thickness.

4 CONCLUSIONS

Double gate SOI devices with ultra-thin silicon and gate oxide films have been investigated on the process related V_{TH} variation. We would like to conclude that double gate SOI MOS structures are promise in preventing SCE. However, the film thickness, channel length, oxide thickness, and doping profile must be carefully optimized to reduce the influence of V_{TH} variation, especially for nanoscale devices. From the fabrication point of view, we have to pay attention to the implementation of film thickness, doping profile, geometry, and its corresponding circuit design for the challenge of threshold voltage variation.

5 ACKNOWLEDGEMENTS

This work is supported in part by the TAIWAN NSC grants: NSC – 92 – 2215 - E – 429 – 010, NSC – 92 – 2112 – M – 429 - 001, and NSC – 92 - 815 – C – 492 – 001 - E. It is also supported in part by the grant of the Ministry of Economic Affairs, Taiwan under contract No. 91 – EC – 17 – A – 07 - S1 - 0011.

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