Microcap Selective Packaging through Flip Chip Alignment

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ABSTRACT

In this study, the technique of microcap selective bonding for 3-D microstructures using MEMS processes was presented. The flip-chip assembly was successfully demonstrated that the microcap transferred on the selective area of the host substrate through wafer level alignment. A new packaging technique of microcap with passivation treatment was developed for selective packaging. The metal Ni microcap is superior to those using thin film poly-silicon by surface micromachining technique due to the high stiffness structure. Photo definable material was served as the bonding adhesive layer between the silicon wafer and metal microcap. For the bonding process, several types of photo definable material were explored to characterize for bonding strength. The result shows that excellent bonding strength under bonding temperature can be achieved.

Keywords: flip-chip, passivation, microcap, wafer level, MEMS process

1 INTRODUCTION

One major cost driver in today's MEMS is the packaging process. MEMS includes moving structures, requirements for packaging of such components must take that into account. Some functions also include interaction with the surrounding environment, such as pressure sensors. Packaging should provide mechanical support to the sensitive chip.

MEMS Packaging includes wafer bonding processes and microfabrication. There are several wafer bonding techniques offering permanent wafer protection, such as anodic and fusion bonding. Conventional anodic and fusion wafer bonding techniques can not be employed to all MEMS and IC bonding process due to high temperature or high electric fields during the bonding process, which might damage IC or MEMS devices. These problems have prompted researchers to study low-temperature bonding techniques, and use eutectic bonding .

A process of selective encapsulation with low temperature bonding technique was presented, including localized silicon-gold eutectic bonding, localized silicon-glass fusion bonding, localized solder bonding and localized CVD bonding processes. There are also methods such as the donor/target procedure, using two wafers, one for the micromechanical component and one for the MEMS component. Hermetic packaging of microdevices devices is required in many applications. Resonant, and tunneling devices, infrared and pressure sensors, voltage controlled oscillators and vacuum displays all utilize vacuum sealing to improve performance. Vacuum sealing can be accomplished at the package level using brazing, soldering or welding. Wafer-to-wafer bonding has also been employed to hermetically seal microdevices. However, these approaches require bonding temperature over 220 °C to finish the process. Although the temperature is much lower than that of anodic and fusion bonding, still, it will damage some of the IC and MEMS structures during the bonding process. Another encapsulation method fabricated by MEMS process was developed. Glass wafer was etched to accommodate the microcap. Besides, the transparent characteristics of glass wafer will facilitate the alignment process during bonding. But, glass etching is time consuming and loose of precision. It would be very advantageous if a first-level or device-level packaging were performed in such a way that the remaining packaging procedures for MEMS chips would be the same as those for IC chips using common procedures with existing IC packaging equipment.

In order to accomplish these goals, we use flip chip and wafer level alignment to batch fabrication to lower the manufacturing cost, to fabricating encapsulation with passivation technique to protect MEMS devices, and to offering lower temperature and electric field free bonding process to prevent the IC and MEMS devices from thermal damage and exploring various photo definable material to find the strongest bonding strength. Furthermore, the passivation techniques were utilized in transferring microcap on the selective area of the host substrate. The process flow of wafer level bonding using flip chip packaging is shown in figure 1. Photo definable material with patternable characteristics was served as the bonding adhesive layer between the microcap and host wafer. Bonding experiment with several types of photo definable material were explored for bonding process. It shows that excellent adhesion strength between microcap and host wafer can be obtained.

2 BONDING PROCESS

The wafer bonding process can be divided into following steps: First, the metal microcap is fabricated on the carrier substrate with passivation treatment. Then wafer level and flip chip method was used to transfer the metal microcap selectively on the host substrate. Finally, two

wafers were separated. The metal microcap will be transferred on the selected area of the host substrate. The bonder used in the study is a commercially available EV501 (Electronic Visions) with PC controller. AZ-4620 (a positive photoresist from Shipley), JSR-137N (a negative photoresist from Japan Synthesis Rubber Co.), SU-8 (a negative photoresist from Microchem Co.), and SP-341 (a positive photoresist from Toray Co.) were selected as bonding adhesive layer material for the bonding experiments.

2.1 Fabrication of the metal microcap

For the fabrication process for the metal microcap. Four-inch (100) single side polished silicon wafer with 525 μm in thickness was used. Oxide is grown thermally with a thickness of 1.5 μm at 1050 ^{o}C. After etching mask was defined on the carrier silicon wafer. The silicon is anisotropically etched using 30 wt% KOH at 70 ^{o}C to form a cavity. This etchant does not attack the silicon oxidation. The cavity is formed by the (111) silicon surfaces which etch at a much lower rate than the (100) surfaces in the anisotropic etchant. The exact shape is defined by the edges of the pattern due to orientation-dependent etching, and the (111) surface forms an angle of 54.74 ^{o}. A Ni layer of thickness 150nm is then sputtered functioned as seed layer for electroplating, followed by a passivation treatment on its surface. Later the Ni layer with passivation treatment will help the metal microcap to separate from the carrier substrate. Then a thick photoresist was spin coated to form the electroplating template for the metal microcap structures. Ni metal microcap structure with 15 μm in thickness can be formed by electroplating process. Therefore, the metal Ni microcap is superior to those using thin film poly-si by surface micromachining technique due to the high stiffness structure. Then, another photo definable material was coated onto the surface of the silicon wafer. To evaporate the solvent contained in the photo definable materials, the material was baked for a period of time. The sample was then exposed and developed to define the bonding pad on the metal microcap. Finally, the electroplating template was removed.

2.2 Flip chip and wafer level bonding

The flip chip method was used to transfer microcap on the selective area of the host substrate through wafer level alignment. These two wafers were then placed into the bonder. During the bonding processing, the temperature was adjusted based on the adhesive layer material. The bonder allows wafers to contact and be annealed between plane heaters. The final procedure is to remove the carrier silicon from the host silicon wafer. After the carrier silicon wafer is pulled upwards, the microcap will be separated form carrier silicon wafer, and leaving the microcap on the host substrate. It is worth noting that the metal microcap can be easily separated from carrier substrate because the Ni layer on the carrier wafer has a passivation treatment in advance. The process of passivation treatment is to put the Ni layer into oven flushing with air under a period of time. The chart of time vs. temperature for the treatment is shown in figure 2. And due to the treatment, the carrier substrate can be reused to fabricate metal microcap. In this approach, the bonding process allows transferring microcap on the selective area of the host substrate. MEMS device can be protected by the metal microcap. This method is particularly suitable for the integration of micro-structure with microelectronics involved in MEMS packaging. Once the microcap is transferred on the host wafer, the microdevices are then protected, and can be treated as same as an IC wafer during subsequent dicing. Devices can be batch-fabricated and batch-packaged. Individual packaged microcap-base chip can then be obtained by dicing along dicing line. The individual MEMS device with microcap which can be diced as standard IC dicing process. The microcap from of 50μm 50μm to 1.5mm x 1.5mm in area can be made to protect microdevices.

2.3 Bonding inspection

The common measurement techniques are bond imaging, cross-sectional analysis, and bond-strength measurement. The bond imaging methods are nondestructive and can be used as in-process monitors, while the cross-sectional analysis and bond strength measurements are destructive for characterization.

Infrared (IR) transmission was setup to inspect the bonding structure. It consists of an IR source and an IR sensitive camera with excellent sensitivity in the near-IR range. The bonded wafer pair is located between the source and camera. Any defect after the bonding will show up. Examples of the images obtained by the method for two bonded 4-inch silicon wafer pairs are shown in figure 3. It shows the method can successfully examine bonding result. The bonding pad can be clearly identified as shown in figure 3 (a). On the other hand as shown in figure 3 (b), if Newton's Ring appears, it means void or defect existing in the bonding area. This imaging method generally cannot image voids with a dimension less than one quarter of the wavelength of the IR source.

2.4 Low temperature and electric field free bonding

Photo definable material was applied as the intermediate adhesive layer in this bonding process. It has several features; low bonding temperature, electric field free, strong bonding strength and excellent surface planarization properties. In the experiments, the single polished silicon wafers were bonded with other Ni coated wafer using different photo definable materials. The influences of the bonding material, the bonding force, and the bonding temperature were investigated.

The bonding pad can be patterned on the silicon wafer through photolithography. Therefore, its resolution can reach as small as 5 μm. The result shows that the adhesive layer can adhere on the bonding surfaces firmly to increase the bonding strength.

The bonding temperature around 50 ~ 150 °C was tested. When the adhesive layer material reaches the pre-set bonding temperature, it causes the interface of the two wafers bonded tightly, and forming excellent bonding strength. For the tensile strength test, bonded pairs are cut using dicing saw. The bonding chip is attached using a clamping apparatus in the MTS (Material Test Station) for the bond strength test. The clamping apparatus is pulled apart using a selected pull force and speed.

3 RESULTS AND DISCUSSIONS

The curves for the bonding strengths are shown in figure 4. Each data represents the average of three measurements. Figure 4 shows the tensile test curves as a function of bonding temperature under a constant bonding force (50N). From the result, it can be seen that when the bonding temperature for SU-8, JSR, AZ-4620, and SP-341 was between 80 °C and 100 °C, the bond strength reached their maximum. When the bonding temperatures were higher than 140 °C, AZ-4620 would be scorched. Besides, if the bonding temperatures were higher than 200 °C, SU-8, JSR, and SP-341 exhibited the same bonding strength as at 100 °C. It also shows that SU-8 used as adhesive layer under bonding temperature 90 °C has maximum bonding strength about 213 Kg/cm^2 (20.6 MPa). SU-8 has many attractive properties as an intermediate adhesive layer described as follows. SU-8 has an epoxy feature with very high bonding strength. SU-8 is a negative photoresist and is crosslinked after exposed to UV light. It exhibits increased chemical resistance after UV exposure. In addition, it just requires very low bonding temperature 90 °C to form excellent bonding strength. On the other hand, as for AZ-4620, when the bonding temperature was about 90 °C, the bonding strength reached about 86 Kg/cm^2. When a thinner bonding pad is required, the AZ-4620 photoresist is a good choice for the bonding process. Regarding SP-341, when the bonding temperature about 90°C, the bonding strength of SP-341 would be about 100 Kg/cm^2. When the bonding temperature for JSR was about 90 °C, the bonding strength reached about 88 Kg/cm^2.

The bonding temperatures of 90 °C for SU-8, JSR, AZ-4620, and SP-341 were tested. The result shows that when the bonding force was reduced, the bonding strength became weak between the two wafers because of voids created by the uneven wafer surface and by the voids trapped in photoresist. It is worth noticing that with a lower bonding force, the bonding between the substrate and intermediate adhesive layer can not be formed tightly because the bonding force is not strong enough to eliminate the void and gap in the interface. Besides, when larger bonding force is applied, the adjacent microstructure and IC may be destroyed. The selection of bonding force is an important parameter in the bonding processing. The bonding force is very important factors in wafer bonding technology.

It has been shown that when the bonding strength reached their maximum about 80~210 Kg/cm^2, respectively. The maximum strain of SP-341 is 155E-3, SU-8 is 80E-3, AZ-4620 is 70E-3, and JSR is 60E-3. It is worth noticing that SU-8 will become ductile behavior in the interface after bonding, but the intermediate layer using SP-341 will show elastic characteristics after bonding. The choice of intermediate layer can be based on the requirement of bonding process.

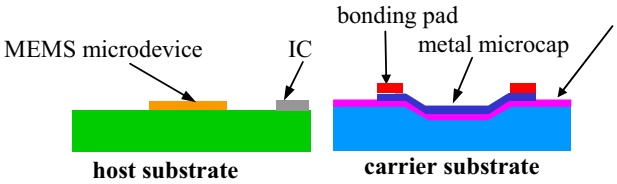
Thickness of adhesive layer less than 20 μm can be achieved (see figure 5). The thickness of the intermediate adhesive layer can be controlled precisely by the spin-coating process. Due to photolithography process, the lateral width of bonding pad can be controlled down to 10μm. Therefore, the bonding has great potential for substrates with higher density of IC and MEMS devices.

4 CONCLUSION

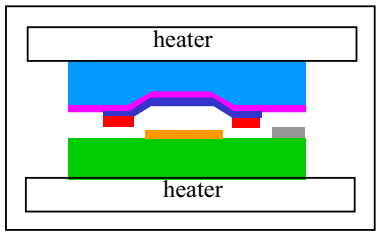
In this study, a silicon wafer bonding technique for 3-D microstructures using photoresist as adhesive layer was presented. The flip chip and wafer level bonding were successfully utilized in demonstrating the transferred microcap on the selective area of the host substrate. Passivation technique can help the metal microcap separating from carrier wafer. Ni metal microcap structure with 15 μm in thickness can be formed by electroplating process. Therefore, the metal Ni microcap is superior to those using poly-si by surface micromachining technique due to the high stiffness structure. The micro encapsulation with passivaton treatment can be used as a new packaging technique. Photo definable material with patternable characteristics can be served as the bonding adhesive layer between the silicon wafer and microcap. Several types of photo definable material were tested for bonding strength. Resolution of bonding pad and thickness can be down to 10 μm and 20 μm, respectively, which is very suitable for high dense IC and MEMS packaging. The results indicated that SU-8 is the best material with bonding strength up to 213 Kg/cm^2 (20.6 MPa) under 90 °C bonding temperature. When bonding is required of a high resolution bonding pad, strong bonding strength, electric field free and low temperature bonding technology, the best solution is to use photo definable material as the bonding adhesive layer. It can offer an excellent bonding result.

5 ACKNOWLEDGEMENT

The author would like to thank the National Science Council of the Republic of China for its support of this work with Grant No. NSC-92-2212-E-110-029.



(a)



flip chip and wafer level alignment in vacuum environment

(b)

bonding process

(c)

microcap transferred on selective area

(d)

Figure 1 Process flow chart of flip chip and wafer level bonding with microcap protection

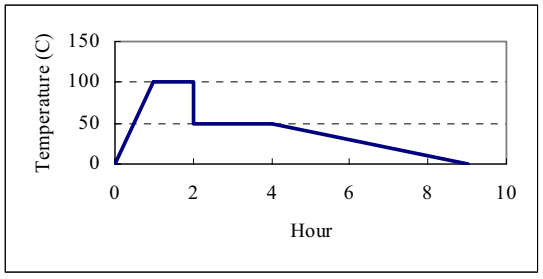
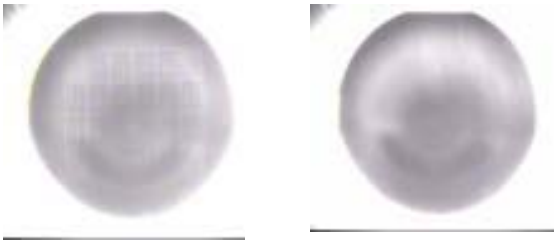


Figure 2 Chart of temperature vs. time for passivation treatment



(a) successful wafer bonding (b) failed wafer bonding with void

Figure 3 IR transmission image of two bonded wafer pairs

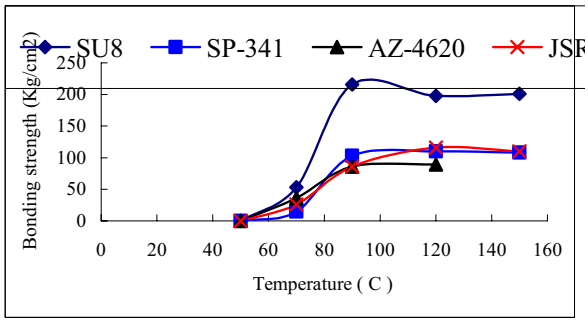
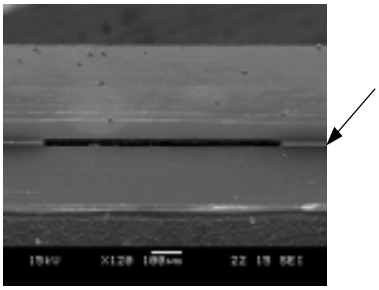
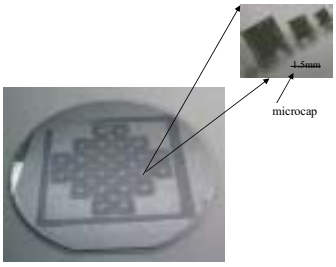


Figure 4 Experimental result of bonding strength and bonding temperature for various intermediate adhesive layers



Thickness of adhesive layer less than 20 µm



Microcap on selective area

Figure 5 Experimental result of microcap bonding