Hierarchical Simulation Approaches for the Design of Ultra-Fast Amplifier Circuits

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ABSTRACT

The silicon-on-insulator (SOI) technology is one of the most promising technologies as the semiconductor industry shifts to 0.13μm and smaller devices. Fully depleted (FD) SOI transistors offer a nearly ideal behavior for application in analog circuits, particularly in high frequency and low power operation. In this work, the design and development of a highly efficient power amplifier circuit is investigated for SOI technology. A fully depleted NMOS SOI transistor is built and characterized, which exhibits TeraHertz cutoff frequencies. The device parameters of this transistor are then extracted to build a compact circuit model for use in the PSPICE circuit simulator. Finally, a low power and high frequency class E power amplifier is designed based on the SOI transistor, and a full analysis of the performance compared to bulk Si technology is performed.

Keywords: FDSOI, DST, class E power amplifier, power-added-efficiency, drift diffusion

1 INTRODUCTION

The inherent characteristics of SOI based structures improve device speed by 15% to 35% over that exhibited by bulk CMOS technology [1]. Previous works demonstrate the advantages of SOI in low power digital baseband circuits such as microcontroller CPUs, SRAM, DRAM and ALU [2]. More recently, results of receiver functions such as low noise amplifiers, mixers and VCOs implemented in SOI have been reported. Lack of successful demonstration of a power amplifier has been one element preventing implementation of a complete SOI RF transceiver [3]. In battery-operated devices like cell phones, the talk time directly depends on the efficiency of the power amplifier (PA) in the transmitter. Input power consumption of other blocks in the transceiver (DSP/baseband circuitry, oscillators, mixers, filters, LNA etc.) is often negligible to that of the PA and much research is focused on how to improve the efficiency of PA circuits.

Currently, bulk Si MOS technology is the dominating technology in the semiconductor and integrated circuit industry. The main goal in this work is to investigate the performance of the class E PA circuit built on SOI technology. The n-channel SOI transistor designed here is based on the DST transistor [4] fabricated by Intel. Model parameters are extracted from the simulation data of the device in order to build a compact circuit model of the SOI transistor for use in the class E PA circuit.

2 DEVICE CHARACTERIZATION

The circuit design process begins with the modeling and characterization of a 70nm fully depleted SOI NMOS transistor. Figure 1 and Fig. 2 show the schematic layout of the simulated device and the corresponding electric potential profile, respectively. Where available, the internal device parameters correspond to the values of the DST transistor fabricated by the Intel group [4]. The sub-70nm transistor consists of a thin silicon body 30nm thick fabricated on top of a 200nm thick buried oxide. The physical gate oxide thickness is equal to 1.5nm.

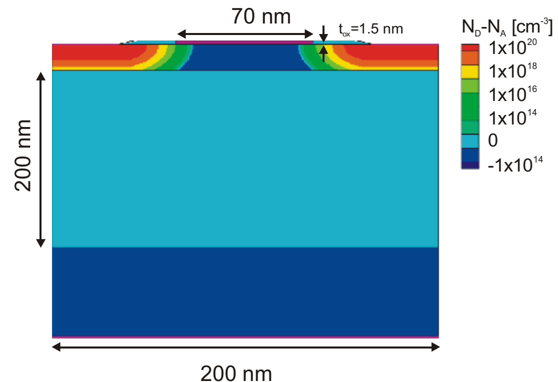

Figure 1: Schematic layout of FDSOI device simulated with the DESSIS

The device is simulated with both a fullband particle-based simulation tool [5] and with the ISE-TCAD drift-diffusion simulation tool, DESSIS [6]. Figure 3 shows the corresponding I-V curves of the device simulated with the drift diffusion transport model. The on current is found to be 0.75mA/um at V_{dd} = 1.3V compared with 1.18 mA/um in the DST device. This is due to the fact that the experimental device has a raised source and drain contact region that improves the on current by 20% [3]. The computed saturation current is also higher than the experimental values, and this discrepancy can be attributed to the lack of experimental information available about the doping profile and the source and drain contact resistances.

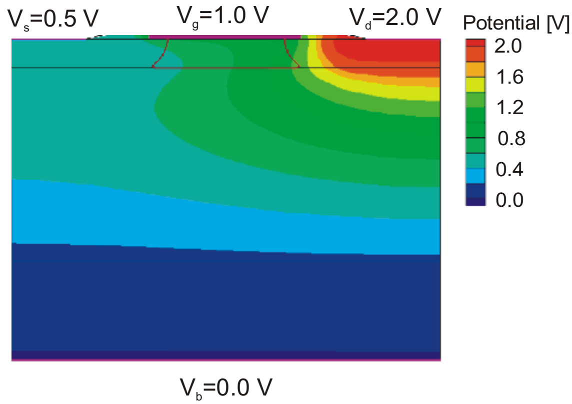

Figure 2: Potential profile for V_{gs} = 1.0V and V_{ds} = 2.0V

The DST transistor is reported to have an operational frequency in the TeraHertz range [3]. The frequency analysis of the device was conducted with both the particle-based simulation tool and DESSIS to further calibrate the proposed FDSOI structure. Within the particle-based approach, a constant bias was applied to the gate electrode while a step voltage was applied at the drain. The drain current was recorded and the complex impedance was obtained as a function of frequency, following the approach of [7]. The results show a cutoff frequency of approximately 1 THz. To further verify the frequency behavior, ISExtract [6] was used to extract the small-signal model parameters of the FDSOI device. The parameters were then used to build the equivalent circuit in PSPICE and the frequency response was then recalculated. Figure 4 shows the plot of the frequency response of the device obtained from the PSPICE simulation. It can be seen that the 3 dB frequency is approximately 1 Thz.

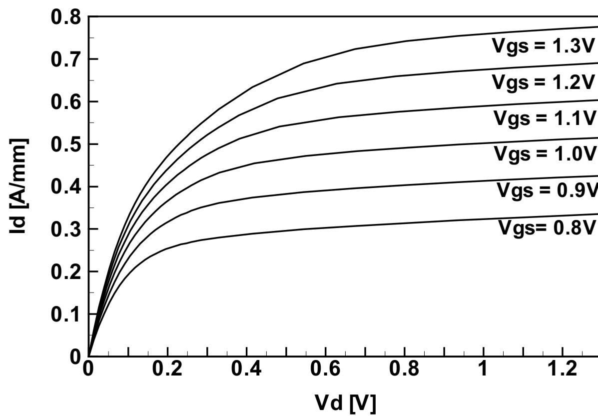

Figure 3: Output characteristics of the FDSOI transistor presented in the above figures

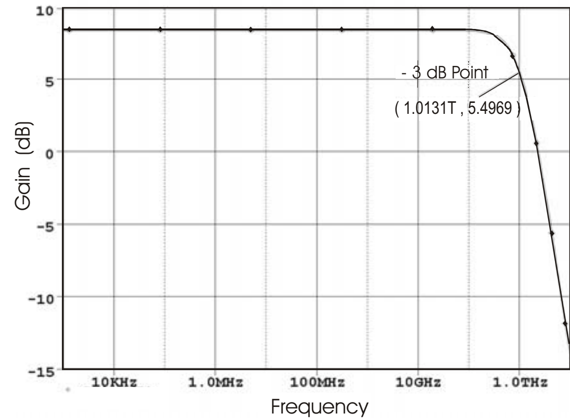

Figure 4: High frequency response of the SOI device

3 CLASS E POWER AMPLIFIER

The high frequency operation of the simulted FDSOI transistor makes it particularly well suited for analog applications. The FDOSI device is used to build a class E power amplifier to show the performance improvement over bulk Si technology. Class E power amplifiers were introduced by Sokal and Sokal in 1975 [8]. These types of amplifiers belong to the switching type of PAs rather than the conventional PAs, where transistors operate as voltage controlled current sources. The final circuit of class E PA is shown in Fig. 6. The output stage consists of a switch, which is the FDSOI transistor, a grounded capacitor C, and a high order reactive network composed of a series combination of inductors and capacitors. The radio frequency chock (RFC) simply provides a DC path to the supply and approximates an open circuit at RF. The capacitor C is placed in such a way that it can absorb any device output capacitance. The reactive network reduces the switch loss by forcing a zero voltage and a zero slope at the turn-on of the switch [9]. The idea behind the class E PA is to employ non-overlapping voltage and current waveforms to improve the power efficiency. Hence, the transistor in this configuration is treated as a switching device. In the case of negligible switching loses the circuit efficiency approaches 100%. However, the switching operation makes the PA highly non-linear and it requires extra circuitry to linearize its operation when the input waveform does not have a constant envelop [10]. The non-linearity is a trade-off with high power efficiency, a relative simple design, a high tolerance to circuit variations and a small number of required components.

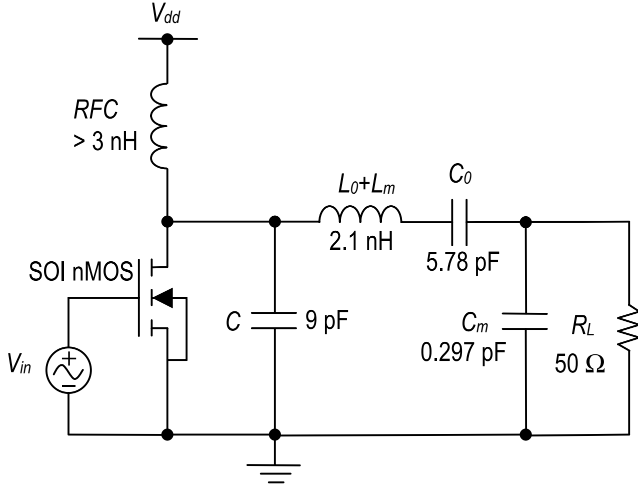

Figure 6: Class E Power Amplifier Circuit

A unique feature of the class E circuit is known as "soft switching", which describes the non-overlapping current and voltage waveform, and results in an efficiency of 100% in the ideal case [10]. The load resistance required for "soft switching" is [9],

$$R_{load} \approx 0.577 \cdot \frac{V_{DD}^2}{P_o} \quad , \tag{1}$$

where V_{DD} is the supply voltage and P_o is the desired output power. It should be noted that R_{load} given by the above equation does not actually match the actual load resistance at small V_{DD} and a transformation network is employed to effectively transform the load resistance to the equivalent resistance. In Fig. 6, the inductor L_m and capacitor C_m represent a simple *L-match* network for the downward transformation of the load resistance.

The proposed power amplifier (PA) is designed for operation at 1.95GHz Universal Mobile Telecommunication System (UMTS) transmission frequency with the target output power of 500mW. Here, the frequency 1.95GHz corresponds to the central frequency of the UMTS uplink band 1920 MHz -1980 MHz [10]. Transistor sizing is an important issue for hand-held devices, and a initial step is the PA design. In the simulated circuit design, the device was sized to obtain the desired output power and to avoid unrealistic high current densities that could give reliability problems. This means that the FDSOI transistor must be fairly large to provide low on-resistance, and to minimize the losses during the on state. The performance of the class E PA is measured by two quantities, namely, drain or output efficiency and power-added-efficiency (PAE). The drain efficiency of a power amplifier is defined as,

$$\eta = \frac{P_{out}}{P_{dc}} \quad , \tag{2}$$

where P_{out} is the output RF power and P_{dc} is the supply power. While PAE is given by,

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad . \tag{3}$$

PAE takes power gain into account and simply replaces the RF output power with the difference between the output and input power in the drain efficiency equation. Here, P_{in} is the input power for the power amplifier. In this design the input terminal of the transistor is driven by a sinusoidal voltage source, although the ideal driving signal for a class E PA is a squarewave or trapezoidal voltage [10]. At GHz frequencies it is difficult to efficiently generate such pulses and hence a sinusoidal driving signal provides a good approximation and a realistic option. A similar circuit design is found in literature [10] with three different technologies. Table 1 compares the performance of the class E power amplifier built with the FDSOI with that of BJT, HBT and CMOS technologies.

Table 1: Comparison of results for four Class E Pas

Parameters	Technology			
	Results from [Mil03]			Results from This Work
	BJT	HBT	CMOS	SOI
Frequency (GHz)	1.95	1.95	1.95	1.95
Supply Voltage (V)	3	3	1.2	1.2
Output Power (mW)	498	482	410	492
Output Efficiency, η (%)	79	89.6	79.6	97.8
PAE (%)	75	86	-	88.1
Power Gain (dB)	13.5	14.3	-	10.04

It can be seen that the SOI technology achieves the highest drain efficiency and PAE. The drop in the efficiency from the theoretical 100% value is caused by several factors. A transistor can only approximate the switching action and will exhibit finite turn-on and turn-off transitions. Thus, there will be a certain overlapping of non-zero voltage and current that will introduce losses. Due to the excellent speed performance characteristics of SOI transistor, the turn-on and turn-off transition times are greatly reduced, which in turn contribute to higher drain efficiency and PAE.

Studies were also conducted on a 3D tri-gate FDSOI structure, which are based on the 25nm Omega FET [11]. These devices represent an attractive alternative to the FDSOI because they show superior scalability, both from a reduction in short-channel effects and an improvement in the gate control over the channel [11]. The simulated tri-gate structure and the corresponding potential profile are shown in Fig. 7 (a) and (b), respectively. Further simulations are being run to characterize the tri-gate FET and extract the small signal parameters for use in the amplifier circuit.

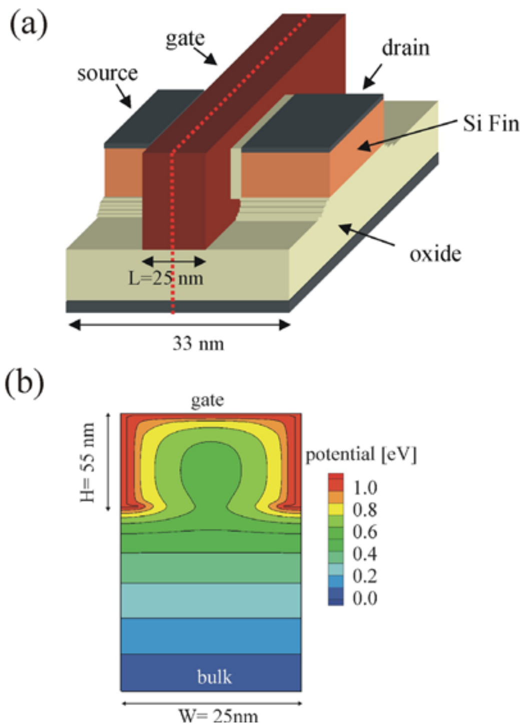

Figure 7: (a) Schematic layout of 25 nm CMOS Tri-gate FET and (b) corresponding potential profile for a gate and drain bias of both 1.0 V.

4 CONCLUSION

In this paper he performance of class E PA operation based on SOI technology is studied. A fully depleted 70nm SOI NMOS transistor is characterized and simulated in order to obtain the compact circuit model of the transistor. The class E PA circuit is then designed based on the SOI device and simulated. Simulation results show that PA has 97.8% drain efficiency and 88% PAE. However, the results should be adopted with caution as ideal passive components have been used. A similar design can be found in [10] for BJT, HBT and bulk Si CMOS technologies and the comparison of results shows that SOI technology significantly improves the performance of the PA.

Acknowledgements

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