Full-band Particle-based Simulation of Germanium-On-Insulator FETs

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ABSTRACT

We model and simulate novel fully depleted (FD) sub-50nm gate lengths MOSFET structures using a full-band particle simulator based on the Cellular Monte Carlo (CMC) method that provides an accurate transport model at the high electric fields present in these nanoscale devices. Simulations of Germanium- and Silicon-On-Insulator devices (GOI and SOI, respectively) are performed to quantitatively investigate the predicted increase of performance of GOI technology. A comparison of static and dynamic properties of similar GOI and SOI devices is performed for 50 nm and 35 nm gate lengths.

Keywords: full-band simulation, SOI MOSFET, frequency analysis, high-κ dielectric, Germanium

1 INTRODUCTION

The general trend of microelectronic technology towards higher circuit integration has driven the size of semiconductor devices into the sub-micron regime; to this end FD Silicon-On-Insulator technology [1] has generated a tremendous interest due to the operating speed, lower voltage and power-consumption in comparison with traditional bulk devices. However, Silicon (Si) inversion layers exhibit asymmetric low-field electron and hole mobilities, resulting in a degradation of the performance of n-channel devices over their p-channel counterpart. This asymmetric behavior is less pronounced in Germanium (Ge), which makes it an attractive material for extending CMOS to sub-micron devices. The higher electron and hole mobilities of Ge also translate into larger saturation drain currents, enhanced transconductance and higher cut-off frequencies [2].

In this work, we model and simulate charge transport in several novel sub-50nm GOI and SOI MOSFETs using a full-band particle-based simulator based on the Cellular Monte Carlo (CMC) method [3, 4]. Simulation of a realistic representation of the layout of such devices is particularly challenging due to the fact that the high doping gradients used in the layout of these down-scaled devices requires extremely fine discretization schemes resulting in a large computational burden. In order to investigate the predicted increase of performance of GOI over SOI structures we compare the transport properties of several GOI and SOI MOSFETs. A preliminary frequency characterization of these devices is also performed through the analysis of their transient response [5].

In the following section, the CMC algorithmic approach is summarized. In Section 3 we present the different simulated GOI and SOI structures. Finally, we compare and discuss the simulation results in Section 4.

2 CMC FULL-BAND SOLVER

The use of a full-band solver is of critical importance to realistically model the devices considered in this work; indeed, analytical approximations of the band structure fail to accurately account for the pronounced warping of the valence bands in Ge and the transport properties at high electric fields that are present in the small structures of interest. The full-band particle-based solver used in this work is based on the CMC approach, which was developed to address the need for computational resources associated with the Ensemble Monte Carlo (EMC) method [6]. This efficient simulation code allows the full characterization of a nanoscale MOSFET structure within a realistic amount of time. This quality is particularly advantageous for the simulation of p-channel GOI structures for which the low effective mass of holes results in the requirement of a time resolution that can be one order of magnitude larger than that used for simulating SOI devices [2]. Within the CMC framework, the electronic structure is computed with the empirical pseudo-potential method [7] inclusive of the spin-orbit interaction, while the full phonon structure is computed with the valence shell model [8]. Both longitudinal acoustic and optical phonon modes are considered in the computation of the deformation potential scattering [6], and impact ionization is modeled using an energy-dependent analytical fit of the momentum-dependent anisotropic ionization rates, as done in [9]. Steady-state field-dependent velocity and energy characteristics are calibrated for different materials with scattering parameters reported in literature [6, 10]. The band structure of Si and Ge as used within the simulation code are shown in Fig.1 (a) and (b), respectively.

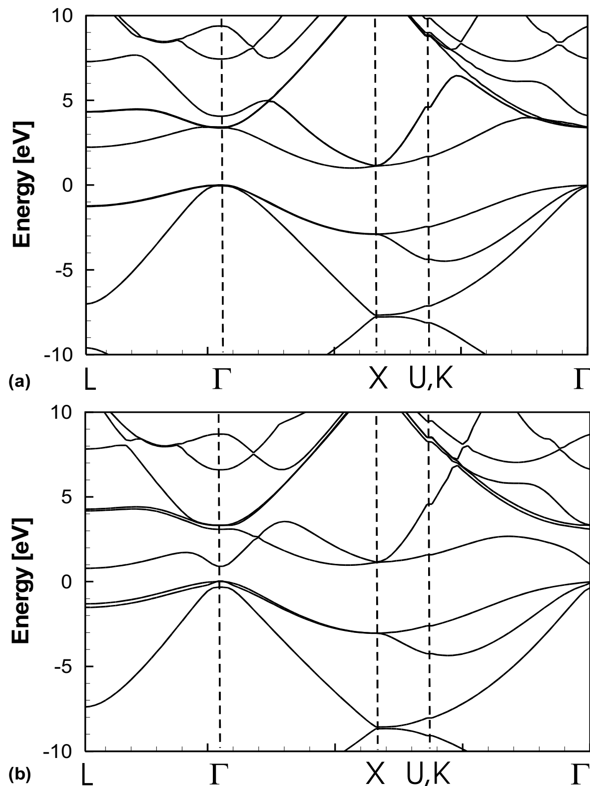

Fig. 1. Representation of the electronic band structure along the L, Γ, X and U,K directions for Si (a) and Ge (b).

3 DEVICE DESIGN AND SIMULATION

To investigate the behavior of GOI FETs, several novel-structure devices have been simulated in this work, including a 50 nm gate, n-channel SOI together with a p-channel SOI and a GOI device with 50 nm and 35 nm gate lengths. For all these devices, the source and drain are separated by 30 nm from the gate ends. A 1.5 nm equivalent oxide thickness layer of high-κ dielectric is used as an insulator between the channel and the gate contact, whereas SiO_2 is used for the 200 nm-thick buried oxide. To ensure full depletion at threshold, a 15 nm doped layer has been simulated in the channel region. A Gaussian doping profile with a peak concentration of 10^{20} cm^{-3} is used in the longitudinal direction, extending 11 nm underneath both sides of the gate. This results in an effective channel length of 28 nm and 13 nm, respectively, for the 50 nm and 35 nm gate structures. The actual layout and doping profile of these devices are shown in Fig. 2 for the 50 nm gate p-MOSFET structure. All devices have been mapped to a 2-dimensional inhomogeneous 256 by 65 grid. Following the standard approach used by particle-based simulation methods [6], the fixed "free flight" time step was set to 0.2 fs whereas the time between successive solutions of Poisson's equation ranged from 10 fs to 0.2 fs depending on the semiconductor material and the doping concentration. Furthermore the use of a very short Poisson time step greatly reduces unphysical oscillations of the output current related to the high doping concentrations in the simulated structures, and facilitates the analysis of the device transient response.

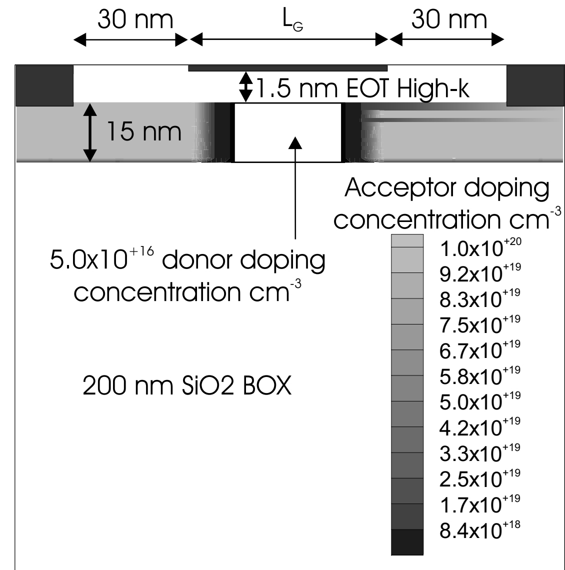

Fig. 2. Layout and doping profile of the simulated devices with L_G = 50 nm

4 RESULTS

4.1 Static Analysis

In Si-based CMOS technology, p-channel transistors are the performance bottleneck due to the lower mobility and saturation velocity of holes.

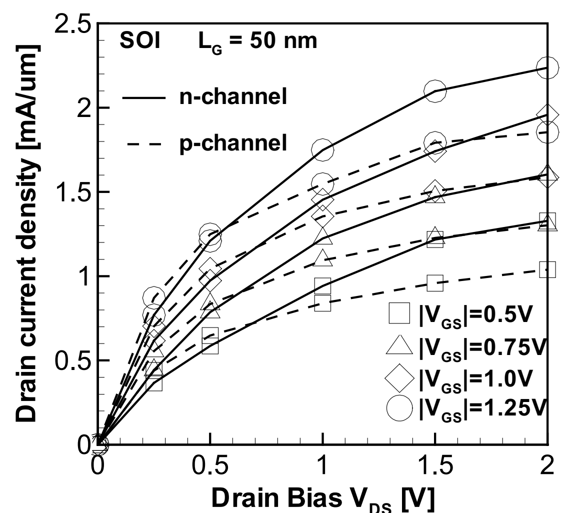

Fig. 3. Comparison of the current density versus drain voltage of 50 nm gate n and p-type SOI MOSFETs.

The resulting degradation of the saturation current in p-type devices is illustrated in Fig. 3, showing the simulated current-voltage characteristics of both p-channel and n-channel SOI MOSFETs with 50 nm gates. The saturation current is 25% higher for the n-channel transistors. In order to study the impact of using similar Ge devices, we compared both GOI and SOI p-channel MOSFETs. Simulation results of the drain current density versus drain voltage for different gate biases ranging from –0.5V to –1.25V are depicted on Fig. 4 (a) and (b) for the 50 nm and 35 nm gate devices, respectively.

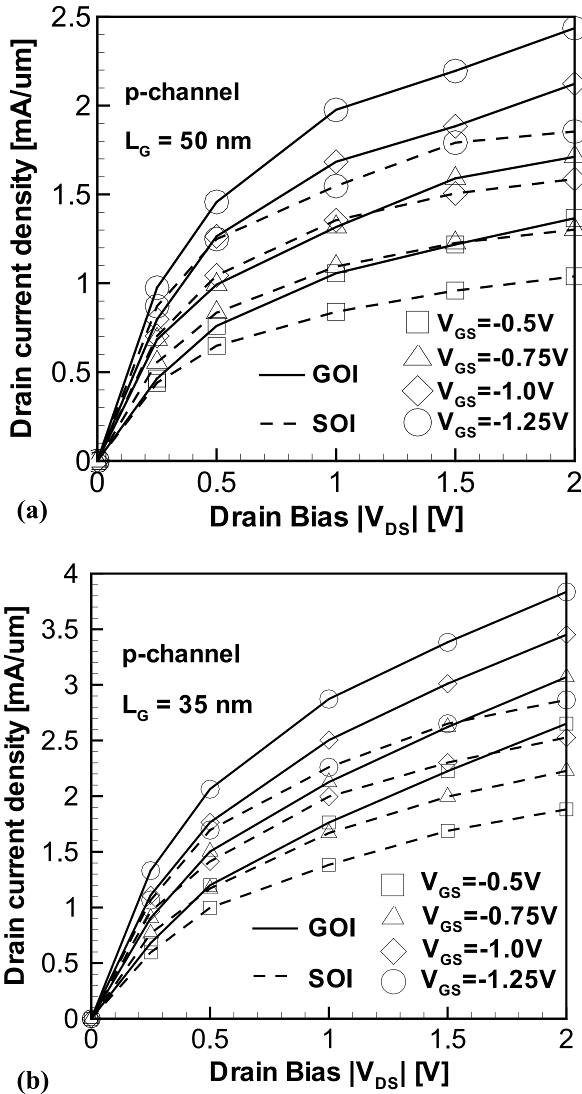

Fig. 4. Current density versus drain voltage comparison of p-channel SOI and GOI MOSFETs for (a) 50 nm and (b) 35 nm gate lengths.

For a drain bias of –2.0V, the observed increase in drain current ranges from 30% to 40% for GOI devices in comparison with SOI technology, which is in agreement with the increased peak velocity of holes inside the channel as shown in Fig.5 for the 35 nm gate p-channel MOSFETs. In both Si- and Ge-based devices, quasi-ballistic transport is achieved in the high field region underneath the gate where the peak velocity of holes is 1.7 times higher than the bulk saturation velocity. In the case of the 35 nm device, the simulated peak velocity of holes is $1.55x10^5$ m/s versus $1.15x10^5$ m/s, which is a 35% increase as shown by the current-voltage characteristics.

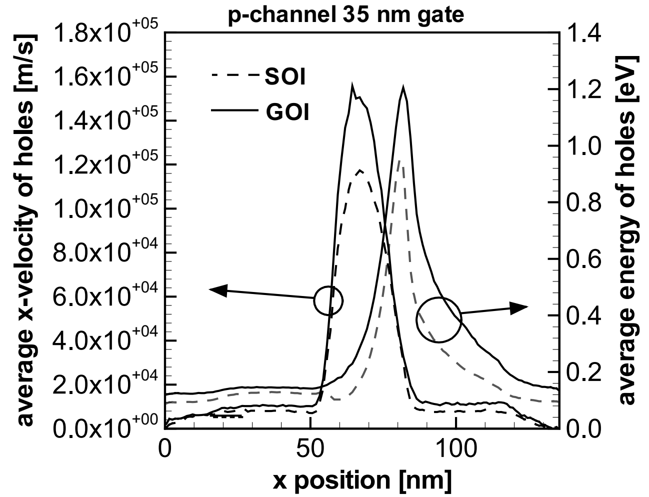

Fig. 5. Average time hole energy and longitudinal velocity along the channel for p-type 35 nm SOI and GOI devices.

The static, DC simulations confirm the expected increase in performance that Ge can provide for CMOS technology. Indeed, the simulated p-channel GOI MOSFETs deliver as much current as n-channel SOI MOSFETs for the same biases, and alleviate the performance differences between p- and n-type Si devices.

4.2 Dynamic Analysis

The frequency analysis of these devices is crucial to study the impact of using Ge on the voltage gain. The method used to investigate the frequency behavior of these devices is based on the Fourier decomposition of the current transients in response to a step voltage perturbation on the drain and gate electrodes. Each device was simulated for 25 ps using a 0.2 fs Poisson time step and 100,000 particles to represent the total hole population, simulation results are typically obtained within 60 hours when performed on a Pentium IV Xeon 2.4 GHz processor. The first 10 ps of the simulation are used to let the device reach steady state about the operating point, then a step voltage on either the gate or drain electrode is applied during the remaining 15 ps. Initial, low resolution results of the voltage gain as a function of frequency are depicted on Fig.6 for the 50nm gate SOI p-channel, n-channel, and the p-channel GOI.

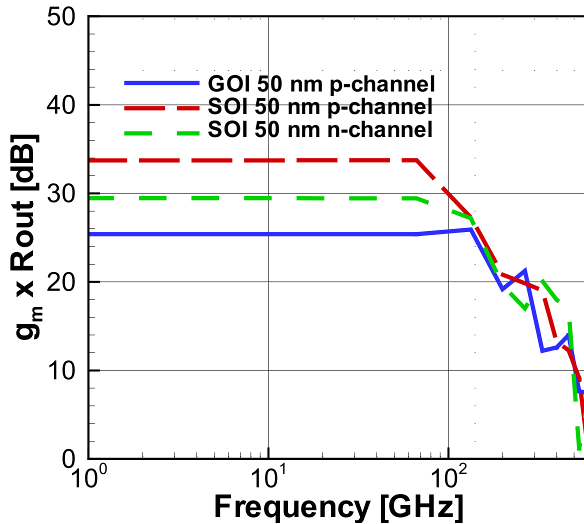

Fig. 6. Voltage gain in dB versus frequency of 50 nm gate GOI and SOI devices.

Within the constant gain bandwidth, the SOI p-MOSFET delivers a relatively higher amplification than the GOI device, nevertheless the –3 dB frequency of the GOI MOSFET is significantly higher than for the p-type SOI device. Longer simulation times will be employed in order to increase the spectral resolution of the present analysis and quantitatively investigate the behavior of these devices within the 30 to 130 GHz frequency range.

CONCLUSION

We have successfully performed a first-hand particle-based investigation of the performance provided by Ge devices used in CMOS technology. The higher mobility observed in Ge with respect to Si translates into higher saturation currents that place p-type GOI MOSFETs on the same performance level as n-type SOI MOSFETs. Similarly promising results have also been obtained with the dynamic analysis. Additional investigation should be performed in sub-threshold regime to further validate the advantages of Ge over Si and confirm GOI as a suitable solution to reduce the performance gap between p- and n-MOSFETs.

ACKNOWLEDGEMENTS

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REFERENCES

[1] J.P. Colinge, “Silicon-On-Insulator Technology: Materials to VLSI, 2nd Edition,” Kluwer Academic Publishers, 2000.

[2] S.M. Sze, “Physics of Semiconductor Devices, 2nd Edition,” Wiley Interscience, 1981.

[3] M. Saraniti, and S.M. Goodnick, “Hybrid Full-band Cellular Automaton Monte Carlo Approach for fast Simulation of Charge Transport in Semiconductors,” IEEE Transaction on Electron Devices, vol. 47, pp. 1909-1915, (2000).

[4] M. Saraniti, J. Tang, S.M Goodnick, and S.J.Wigger, “Numerical challenges in particle-based approaches for the simulation of semiconductor devices,“ Mathematical and Computer in Simulations, 2002.

[5] J. Branlard, S. Aboud, S. Goodnick, and M. Saraniti, “Frequency analysis of 3D GaAs MESFET structure using full-band particle-based simulations,” Proc. of the 9th Int. Workshop on Computational Electronics (IWCE-9), Rome, Italy, June 2003.

[6] M.V. Fischetti and S.E. Laux, “Monte Carlo analysis of electron transport in small semiconductor devices including band-structure and space-charge effects”, Phys. Rev. B, vol. 38, pp 9721-9745, Nov. 1988.

[7] J.R. Chelikowsky and M.L Cohen, “Nonlocal pseudo potential calculations for the electronic structure of eleven diamond and zincblend semiconductors”, Phys. Rev. B, vol 14, pp. 556-582, July 1976.

[8] K. Kunc and O.H. Nielsen, “Lattice dynamics of Zincblende structure compounds-II: Shell model”, Compu. Phys. Commun., vol. 17, pp. 413-422, July/Aug. 1979.

[9] M.V. Fischetti, N. Sano, S.E. Laux, and K. Natori, “Fullband-structure theory of high-field transport and impact ionization of electrons and holes in Ge., Si., and GaAs”, in Proceedings 1996 Int. Conf. Semiconductor Processes and Devices, Tokyo, Japan, 1996.

[10] W. Pötz and P. Vogl, “Theory of optical-phonon deformation potentials in tetrahedral semiconductors”, Phys. Rev. B, vol. 24, pp. 2025-2037, Aug. 1981.