Impact of quantum mechanical tunneling on off-leakage current in double-gate MOSFET using a quantum drift-diffusion model

M.-A. Jaud[1], S. Barraud and G. Le Carval

CEA-LETI, 17 rue des Martyrs
F-38054 Grenoble Cedex 9, France, marie-anne.jaud@cea.fr

ABSTRACT

With the growing use of wireless electronic systems, off-state leakage current in MOSFETs appears as one of the major physical limitations. Measurements of quantum tunnel current between source-drain (S-D) have recently shown that it will become detrim[1]ental in bulk MOSFET architecture for channel lengths around 5nm and at low temperature (≤100K) [1]. In this paper we investigate, using a 2D quantum drift-diffusion model, the influence of source-to-drain tunneling on off-state-leakage current in double-gate MOSFETs.
It is shown that in double-gate MOSFET architecture (contrary to bulk architecture) quantum tunnel current component will be a non negligible part of the off-state leakage current for ultra-thin film thicknesses, even at room temperature.

Keywords: Simulation, density-gradient, Schrödinger, source-to-drain tunneling, off-leakage current, double-gate MOSFET.

1 INTRODUCTION

With the downscaling of MOSFETs into the nanometer regime, the subthreshold electrical characteristics are mainly affected by quantum confinement effects, tunneling current through insulators and source-to-drain tunneling current [1-2]. A measurement of quantum tunnel current between source-drain has recently shown that it will become detrimental in bulk MOSFET architecture for channel length around 5nm and at low temperature (≤100K) [1]. So, to pursue towards low power and high performance circuits, the subthreshold leakage current should be well controlled.
The architecture used in this study is a double-gate MOSFET transistor. This architecture is expected to be a good candidate for ultimate device shrinking, due to its low sensitivity to short-channel-effects and to the improvement of carrier transport properties which is expected from low channel doping [3]. After a careful calibration of quantum drift-diffusion model (QDDM) [4], we present in this paper a systematic study on the impact of source-drain direct tunneling on off-state leakage current in double-gate MOSFET architecture describe in Fig. 1. A large range of temperatures ($100K < T < 300K$), channel lengths ($10nm < L_c < 80nm$) and Si-film thicknesses ($5nm < t_{si} < 15nm$) are used. We show that in double-gate MOSFET architecture (contrary to bulk architecture) the quantum tunnel current component will be a non negligible part of the off-state leakage current for ultra-thin film thicknesses, even at room temperature.

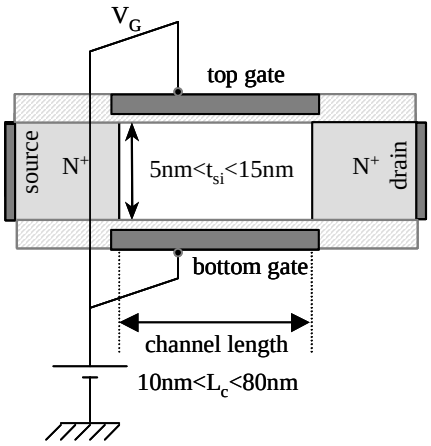

Figure 1: Schematic cross-section of the simulated double-gate nMOSFET (S/D: $10^{20}cm^{-3}$, channel: $10^{16}cm^{-3}$).

This paper is organized as follow : first of all, we demonstrate the ability to model quantum confinement effects with a quantum drift-diffusion model. This model is calibrated with C-V curve simulations in long MOS capacitor in respect of quantum simulations based on 1D Poisson/Schrödinger equations solver (PS). Secondly, Id-Vg characteristics of double-gate MOSFET are simulated using both quantum (QDDM) and semi-classical drift-diffusion (SC) approaches to estimate the ability to model quantum mechanical tunneling with QDDM and quantify its impact on the subthreshold current.

2 MODEL CALIBRATION

In nanoscale devices, the transport of carriers is expected to be dominated by quantum effects throughout the channel. However, the coupling of quantum effects to transport equations is not well established within a consistent conceptual framework [5]. If a self-consistent Poisson-Schrödinger solver is an acknowledged way to

[1] Present employer : STMicroelectronics, F-38926 Crolles

model quantum confinement effects at the SiO_2/Si interface, it is not well suited to a complete treatment of quantum transport because it is too computationally demanding to be used for everyday engineering analysis. Since many years, the Density-Gradient formalism (e.i. quantum drift-diffusion model) appears as an accurate way to include quantum effects to the transport equations [6-7]. The quantum drift-diffusion model introduces lowest-order-effects of non-locality of quantum mechanics through a quantum correction potential added to the classical potential. The electron drift-diffusion current density may be expressed as [4]:

$$J_n = qD_n \nabla n - q\mu_n n \nabla \Psi^Q \quad (1)$$

with

$$\Psi^Q = \Psi^{CL} + \frac{\gamma \hbar^2}{6m_n}\left(\frac{\nabla^2 \sqrt{n}}{\sqrt{n}}\right) \quad (2)$$

where γ is a fit factor which comes from the fact that QDDM is based on a lowest-order-development, m_n is the carrier effective mass, n the electron density, and $\hbar$ the reduced Planck constant. It can be noted that when $\hbar \to 0$, Eq. (1) leads to the classical electron current density. The implementation of this formalism makes this approach simple and attractive for an engineering tool.

A carefully calibration of the QDDM approach has been performed against the results of a Poisson/Schrödinger equations solver (PS). C-V curves have been simulated on a long MOS capacitor with 10Å gate oxide thickness with a channel doping varying from 10^{16}cm^{-3} to 10^{18}cm^{-3}. The effects of confinement on the C-V characteristics are shown in Fig. 2. We plot C-V curves using semi-classical drift-diffusion model (SC) and quantum drift-diffusion model (QDDM) and compare them with results obtained by resolution of Poisson/Schrödinger equations (PS). An excellent agreement is demonstrated between quantum drift-diffusion model (QDDM) and Poisson-Schrödinger solver (PS) with $\gamma = 3.2$ used in all the range of channel doping. The results show higher threshold voltage and lower gate-channel capacitance in accumulation and inversion regimes when quantization effects are included (cf. Fig. 2). The quantum confinement effects below the gate oxide are well-reproduced by QDDM and practically introduced by adding the quantum correction potential (cf. Eq. 2).

To extend the validation of QDDM, it is now applied to very thin silicon films. The carrier concentration has been calculated in long double-gate MOSFETs using both QDDM and PS. A channel length L_c = 800nm has been used to only considered 1D quantum confinement effects with a film thickness t_{Si}, ranging from 50nm to 5nm. The channel doping $N_A = 10^{16}$cm^{-3} is chosen to be the same that the one used in the next section. The resulting carrier density profiles calculated from 1D Poisson/Schrödinger solver (PS) and quantum drift-diffusion model (QDDM) are shown in Fig. 3. Using a single value for γ ($\gamma = 3.2$), the curves exhibit the quantum repulsion of carrier density at the Si/SiO_2 interface due to the wave nature of electrons. A very good agreement is obtained between QDDM and PS approaches. The validation of QDDM has been performed even in a thin-film double-gate architecture (down to 5nm).

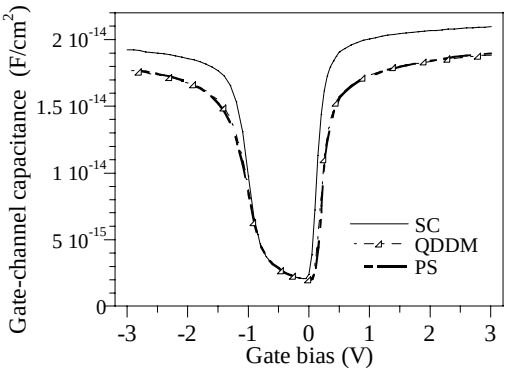

Figure 2: Simulated C-V curves using semi-classical drift-diffusion model (SC), quantum drift-diffusion model (QDDM) and Poisson/Schrödinger equations solver (PS) with a channel doping $N_A = 10^{18}$cm^{-3}.

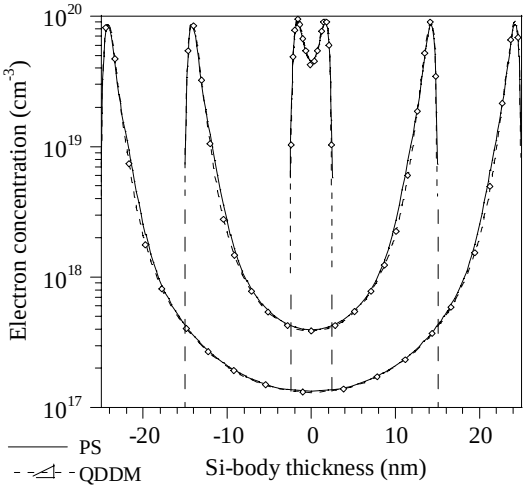

Figure 3: Inversion layer charge distribution calculated from Poisson/Schrödinger solver (PS) and quantum drift-diffusion model (QDDM) with $N_A=10^{16}$cm^{-3}. V_{GS}=1V.

3 SIMULATION RESULTS

The schematic device structure and device parameters used in the simulations are shown in Fig. 1. The source/drain regions and the substrate are doped to $N_D=10^{20}$cm^{-3} and $N_A=10^{16}$cm^{-3}, respectively. To investigate the impact of source-to-drain tunneling on the electrical behaviour of the device, a channel length ranging from 80nm to 10nm and a Si-film thickness ranging from 15nm to 5nm are used. The calculated Id-Vg characteristics are obtained at low drain voltage, *e.i* Vds=10mV using both

quantum (QDDM) and semi-classical drift-diffusion (SC) approaches.

To estimate the ability to model quantum mechanical tunneling with QDDM, we show here the results for a Si-film thickness equal to 5nm. Subthreshold characteristics of double-gate MOSFETs having channel lengths from 80nm to 10nm are shown in Fig. 4. Using semi-classical drift-diffusion approach the subthreshold slope is degraded with the shrinking of the channel length. This degradation can be attributed to short-channel-effects. Using quantum approach (QDDM), results clearly show an increase of leakage current in comparison to SC results as the channel length is decreased (Fig. 4). This electrical behaviour in subthreshold regime is confirmed by results obtained from a full 2D numerical code of quantum ballistic transport including both thermoionic emission and quantum tunneling of carriers [2].

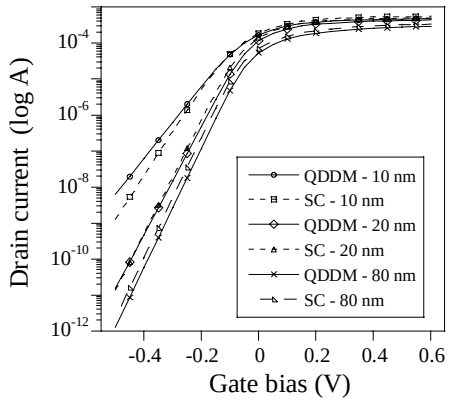

Figure 4: Id-Vg characteristics for a double-gate MOSFET. Comparison is made between semi-classical drift-diffusion model (SC) and quantum drift-diffusion model (QDDM). Silicon film thickness t_{si}=5nm and V_{DS}=10mV.

Indeed, the carriers which come from the source feel steep gradients from the potential barrier. Inclusion of the wave-functions penetration into the barrier is efficiently described with QDDM and induces an additional charge inside the barrier. This charge is self-consistently taken into account in the model and induces a new component to thermal current as observed in Fig. 4. These results show the ability to qualitatively describe the source-to-drain tunneling with a quantum drift-diffusion model.

To consolidate the idea that source-to-drain tunneling is included in the quantum drift-diffusion model, the dependence of subthreshold current on temperature has been investigated. The temperature dependence on Id-Vg characteristics using semi-classical and quantum simulations is shown in Fig. 5 and Fig. 6, respectively.

In comparison to semi-classical drift-diffusion simulations, the subthreshold slope shows a weaker dependence on temperature, which is one of the main properties of measured [1] and calculated [8-10] source-to-drain tunneling current.

Contrary to electrical transport at room temperature, the source-to-drain tunneling plays an important role when the temperature decreases and becomes predominant over the thermoionic current component. These results are in concordance with experimental data [1].

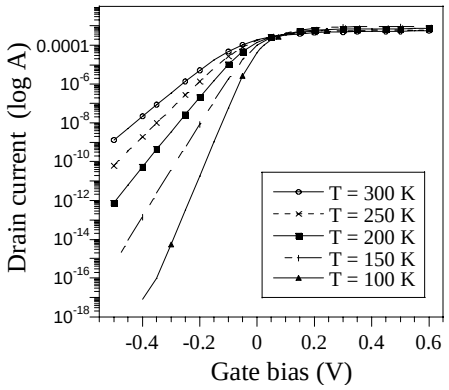

Figure 5: Simulated Id-Vg curves for a double-gate MOSFET with varying temperature using semi-classical drift-diffusion model (SC). Silicon film thickness t_{si}=5nm, channel length L_C=10nm and V_{DS}=10mV.

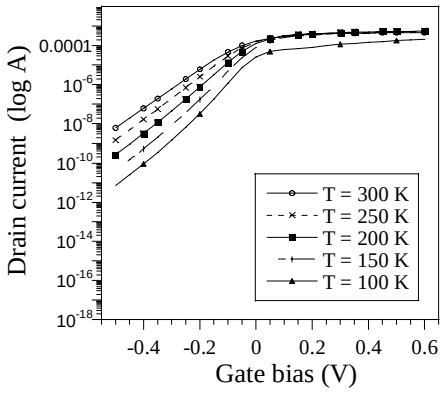

Figure 6: Simulated Id-Vg curves for a double-gate MOSFET with varying temperature using quantum drift-diffusion model (QDDM). The silicon film thickness t_{si}=5nm, channel length L_C=10nm and V_{DS}=10mV.

The relative deviation of subthreshold current calculated at room temperature between QDDM and SC is shown in Fig. 7 for three Si-film thicknesses (5nm, 10nm and 15nm). Two regions may be identified. In the first region 'R1' ($L_c \gtrsim 30$nm), the relative deviation of subthreshold current is essentially due to 1D quantum confinement effects which shift the threshold voltage. In the second region 'R2' ($L_c \lesssim 30$nm) 2D quantum effects characterized by quantum confinement effects and source-to-drain tunneling are present. We show that if quantum tunnelling is not predominant over thermal current for large Si-film thicknesses, a noticeable increase of S-D tunnel current

component appears when the Si-film thickness decreases, even at room temperature.

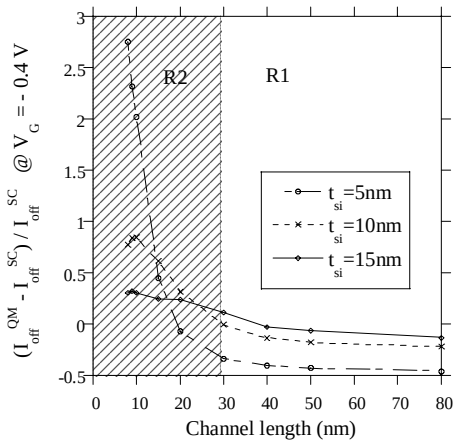

Figure 7: I_{off} relative deviation calculated with quantum drift-diffusion model (QDDM) and semi-classical drift-diffusion model (SC). Regions 'R1' and 'R2' characterize respectively vertical quantum confinement effects and 2D quantum effects. T=300K.

An evaluation of the percentage of source-to-drain tunnel current calculated for different Si-film thicknesses and two temperatures is reported in Fig. 8 with gate lengths ranging from 80nm to 10nm. The calculation is performed for V_{GS}-V_T = -0.2V. As experimentally observed at room temperature, the calculation predicts a thermal current dominant for large Si-film thickness [1]. Nevertheless, it is shown that in double-gate MOSFET architecture quantum tunnel current component will be a non negligible part of off-state leakage current for ultra-thin film thicknesses, at low temperature but also at room temperature.

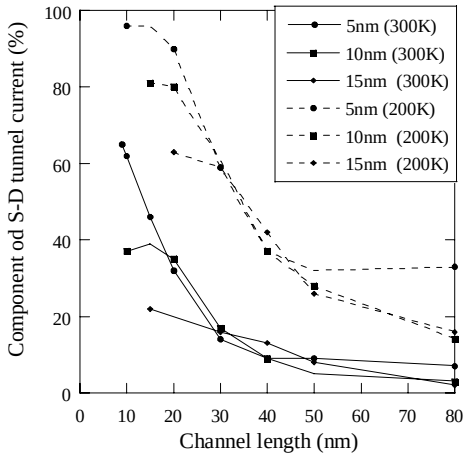

Figure 8: Component of source-drain quantum tunnel current on off-state leakage current (%) for various channel lengths and Si-film thicknesses.

4 CONCLUSION

First of all, we show that a 2D quantum drift-diffusion model (QDDM), based on the Density-Gradient approach, is well-suited to device modelling for which quantum confinement effects significantly affect the electrical behaviour of devices.

Subthreshold electrical characteristics of double-gate MOSFETs with channel lengths ranging from 80nm to 10nm and Si-film thicknesses ranging from 15nm to 5nm have been performed to estimate the ability to model quantum mechanical tunneling with QDDM. For ultra-short channel lengths, a comparison between classical and quantum simulations shows a degradation of the subthreshold slope with inclusion of quantum effects. The additional current induced by QDDM has a similar behaviour to source-to-drain tunnel current (subthreshold slope nearly independent of the temperature) and leads to extend the validation of QDDM to reproduce the source-to-drain tunneling.

We show that at room temperature, the thermoionic current is the main mechanism of electrical transport for large Si-film thicknesses even for short channel lengths (t_{Si}≥15nm and L_c≈10nm). Nevertheless, at low temperature or/and for ultra-thin Si-film thicknesses the influence of tunnel current component has been clearly shown.

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