Scalability and high frequency extensions of the vector potential equivalent circuit (VPEC)*

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Abstract

We present a complete modeling technique for inductive parasitics, based on the vector potential equivalent circuit (VPEC) topology. Novel algorithms for layout extraction and sparsification are introduced. Examples are discussed in terms of CPU time, accuracy, and model complexity. Finally, extensions for high frequency applications are presented, including models for skin effect and full wave simulation.

1 Introduction

Performance estimation of high frequency analog and digital circuits requires the accurate modeling of large numbers of interconnection wires, including their inductive behavior. The widely accepted partial element equivalent circuit (PEEC) technique is based on a dense matrix of inductive couplings, which becomes unmanageable as circuit size grows. Sparsification techniques have been proposed to accelerate PEEC simulations, but they usually involve severe approximations, complex numerical calculations, or even modifications to the circuit simulator [1], [2].

We recently introduced an alternative approach, the vector potential equivalent circuit (VPEC) [3]. The VPEC model mimics inductive couplings by a network of resistive elements and current sources. Unlike the PEEC model, the VPEC topology is intrinsically sparse. VPEC circuit elements have a strong physical interpretation, and can either be derived from first principles, or as the reduction of a PEEC model [4], [5].

In this work we address two issues which are crucial to practical CAD applications, namely, scalability and high frequency modeling. After reviewing the general principles of the PEEC and VPEC models in Section 2, in Section 3 we describe a new layout extraction algorithm which generates a wireframe model. The PEEC model is converted into a VPEC model using an efficient iterative algorithm, described in Section 4. A new model for the skin effect is presented in Section 5, based on a novel direct zero-pole fitting algorithm. Finally, in Section 6, a possible extension of the VPEC model toward electromagnetic (full wave) models are discussed. Conclusions are drawn in Section 7.

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2 The PEEC and VPEC inductance models

The PEEC and VPEC circuit topologies represent two views of the same physical effect, modeled through integral and differential equations, respectively. We start from the equations for the vector potential in the Coulomb gauge:

$$\nabla^2 A_i + \mu J_i = 0, \qquad i = x, y, z. \tag{1}$$

This equation can be integrated to obtain an expression for the vector potential at every point as a function of the conduction current at every other point:

$$\mathbf{A}(\mathbf{r}) = \frac{\mu}{4\pi} \int d\mathbf{r}' \frac{\mathbf{J}}{|\mathbf{r}' - \mathbf{r}|}, \tag{2}$$

Equations (1) and (2) are the starting point for the VPEC and PEEC models, respectively. Integrating Eq. (2) over the wire length, one can obtain the familiar partial inductance equations:

$$V_{em}^k = \sum L_{kl} \frac{dI_l}{dt} \tag{3}$$

where L_{kl} is the partial inductance matrix (PIM) element, which requires the calculation of a double volume integral. Even when acceleration algorithms are used to efficiently compute the PIM entries [6], still the number of matrix entries is proportional to the square of the number of wires, and circuit simulation time explodes for systems with more than a few hundreds of wires. The VPEC model obviates this limitation, since it is based on Eq. (1) rather than Eq. (2). By integrating Eq. (1) over a finite volume Ω^k, one obtains the equation [3]

$$\sum_l \int_{S^{kl}} d\mathbf{S} \cdot \nabla A_i + \mu \int_{\Omega^k} d\Omega J_i = 0, \tag{4}$$

where the sum over l includes all nearest neighbors of Ω^k. This equation can be recast as a Kirchoff current law (KCL) for the circuit of Fig. 1:

$$\sum_l \frac{A_i^l - A_i^k}{R_i^{kl}} + I_i^k = 0. \tag{5}$$

In Eq. (5), the node voltages A_i^k and A_i^l represent the (suitably averaged) i-component of the vector potential in volumes Ω^k and Ω^l. For simplicity, we describe the proportionality between 'magnetic current' and conduction current by a linear

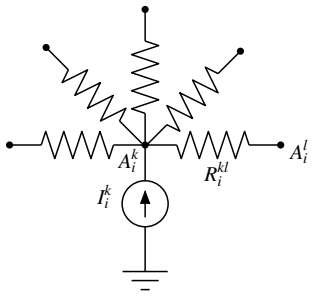

Figure 1: Equivalent circuit for the i-component of the vector potential $\mathbf{A}$. *Voltages* A_i^k *and* A_i^l *correspond to the vector potentials in two neighboring control volumes* Ω^k *and* Ω^l. *Current source* I_i^k *models the effect of conduction current on the vector potential. Resistor* R_i^{kl} *represents the propagation of vector potential between the two regions.*

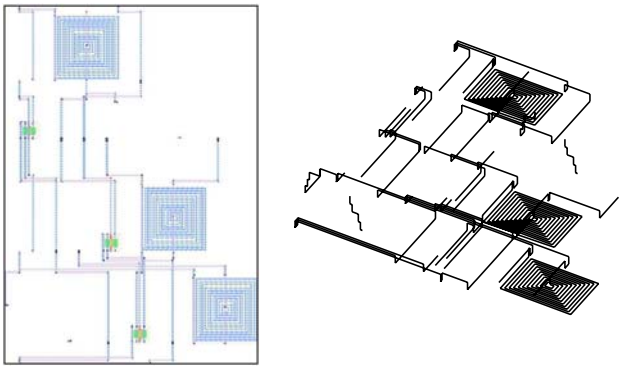

Figure 2: Wireframe extraction from layout. Left: 2D layout. Right: Extracted three-dimensional wireframe representation, which can be fed into FastHenry or other magnetostatic solver.

coefficient F_i^k:

$$I_i^k = F_i^k I_k, \qquad i = x,y,z \tag{6}$$

By the same token, the electromotive force V_k is modeled by a single linear coefficient E_i^k:

$$V_k = \sum_{i=x,y,z} E_i^k \frac{dA_i^k}{dt}. \tag{7}$$

The quantities E_i^k and F_i^k are parameters depending on the wire geometry only and can be easily evaluated [3].

In order to complete the model, one must determine the resistors R_i^{kl} to fit the surface integrals in Eq. (4). Finite-difference approximations, such as those proposed in [5], are much too crude to supply acceptable values for the VPEC resistors. In [3], more refined semi-analytical formulas were proposed based on the extraction methodology of [7]. In Section 4, we will describe a numerical technique that allows the direct extraction of VPEC resistance values from a pre-computed partial inductance matrix.

3 Layout extraction and inductance calculation

Resistance and inductance (*RL*) extraction requires the decomposition of a layout into a set of straight wires with constant cross-section, usually rectangular. Obviously, for general wire shapes, such decomposition is only an approximation. An algorithm for *RL* extraction was presented in [8], based on the identification of elementary rectangular regions which are connected at linear interfaces. We developed a novel algorithm which offers better generality when dealing with complex wire shapes. The algorithm is based on an 'explorer,' i.e., a rectangular shape which moves about the layout, and is completely contained within it. Every time the explorer changes size or direction of motion, a node in three-dimensional space is generated. Wires are generated as straight lines connecting nodes, consistently with the geometric representation adopted by FastHenry [6]. The cross-section of a wire connecting two nodes is given by the size of the explorer, which is by definition constant along the length of the wire This algorithm has the key advantage of being independent of the particular layout representation (rectangular tiles, polygons, etc). Figure 2 shows an example of layout extraction for an RF circuit, including both interconnect wires and spiral inductors.

The wireframe model extracted can be directly fed into a magnetostatic solver such as FastHenry. Since our methodology only needs a subset of the complete partial inductance matrix, we developed a quick extractor using simplified analytical formulas for the partial inductance coefficients. The problem of computing partial inductance matrix for conductors with rectangular cross section was long ago solved exactly in the general case [9]. However the numerical stability of the exact solution is not satisfactory, especially for the case of very long wires [10]. On the other hand, stable simplified expressions are accurate only when the wire length l is much larger than the lateral distance d. We developed a hybrid expression that reduces to the asymptotic form

$$L_{kl}(l,d) = \frac{\mu l^2}{4\pi d}$$

for $d \gg l$, while following the stable simplified expression for $d \ll l$ [9]. The hybrid expression offers an almost exact match to the exact formula, without requiring complex calculations like the model of Ref. [10].

4 VPEC generation

In order to find a way to extract VPEC model parameters from PEEC partial inductances, we note that Eqs. (6) and (7) replace Eq. (3), using the vector potential as an intermediate step between conduction currents and induced voltages. Starting from this observation, it can be shown [3] that the

inductance matrix can be written as

$$L^{lk} = \sum_{i=x,y,z} E_i^l \, \mathcal{Z}_i^{lk} \, F_i^k, \qquad (8)$$

where the quantity $\mathcal{Z}_i^{lk}$ is an entry in the impedance matrix* of the resistive network for the i-component of the vector potential, i.e., the vector potential at node l when a unit current is injected at node k. Under the assumption of equal propagation of vector potential in all three directions $\mathcal{Z}_i^{kl} = \mathcal{Z}^{kl}$, Eq. (8) becomes

$$L^{lk} = \mathcal{Z}^{lk} \sum_{i=x,y,z} E_i^l F_i^k \qquad \text{or} \qquad \mathcal{Z}^{lk} = \frac{L^{lk}}{\sum_{i=x,y,z} E_i^l F_i^k}.$$

From any given wire geometry and PIM, we can immediately determine the VPEC impedance matrix. The VPEC generation problem is then reformulated as *finding the resistors R^{kl} to reproduce a given impedance matrix $\mathcal{Z}$.*

The unknowns in the sparsification problem are the n resistors to ground, plus all resistors connecting neighboring nodes. The calculation of all resistors requires the solution of a very large, nonlinear problem [4]. The size of the problem is due to the fact that the calculation of the impedance matrix requires a full circuit solution (i.e., n equations) for every node in the VPEC. Moreover, the problem is nonlinear, because the resistor values appear in the equations along with the node voltages. The problem can be greatly reduced in size, and linearized, by adopting a block iteration where at each step only the resistors connected to a single node are considered. At each iteration, a very sparse, $n \times n$ linear system results, which can be efficiently solved using standard sparse-matrix methods.

The sparsification algorithm has a complexity around $O(n^4)$, due to the need for solving $O(n)$ systems, each with $O(n^3)$ complexity of matrix inversion. We can reduce this complexity to $O(n)$, by adopting a windowing algorithm that splits a layout into regions which are separately extracted. VPEC models extracted for each of the windows are merged by discarding resistor values at the edges, which will display the largest errors [4]. Figures 3 and 4 report the accuracy and CPU time of the extracted VPEC model. An alternative method for VPEC extraction has been proposed in [5], based on matrix inversion. This approach relies on the fact that for a dense VPEC, where all elements R^{kl} have finite values, the problem of determining resistor values is linear rather than nonlinear. Therefore, the VPEC model is obtained by the inversion of a single $n \times n$ matrix. After VPEC generation, some resistors are discarded based on their magnitude, thus obtaining a sparsified model. This scheme scales with complexity $O(n^3)$, and is therefore potentially faster than the iterative algorithm described above. On the other hand, it requires the knowledge of the entire $n \times n$ PIM, which may pose storage problems of its own. Moreover, even a complexity $O(n^3)$ is too high for large scale circuit extraction, so that some form of windowing will be required anyway.

*The symbol $\mathcal{Z}$, and the term *impedance matrix*, will be employed although the network in question is purely resistive, to avoid confusion with resistor values in the following.

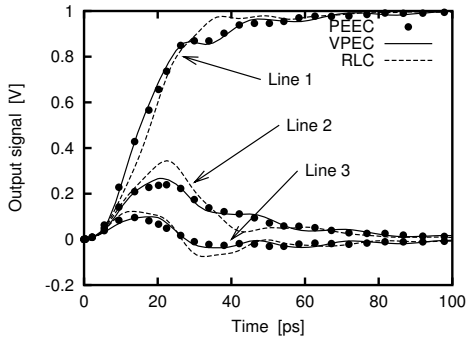

Figure 3: Transient simulation for 32-line bus, when a 1 V, 20 ps step input is applied to the first line. The transient response is shown at the far end of the first three lines.

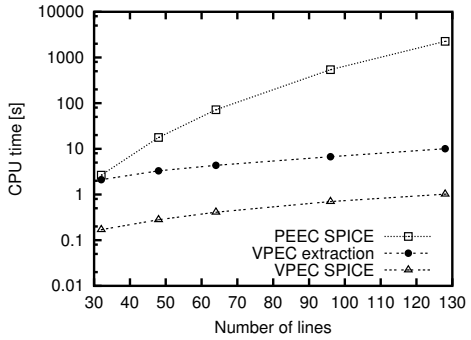

Figure 4: Total CPU time needed for extraction and simulation of a parallel-line bus, with two segments per line, as a function of the number of lines. All simulations were performed using HSPICE on a 2 GHz Pentium-4.

5 Skin effect

In the multi-gigahertz frequency range, skin effect causes current to flow only at the surface of conductors, leading to a decrease of wire inductance and an increase of resistance. The latter effect causes a signal attenuation which increases with frequency, thus limiting the available interconnect bandwidth. Existing skin effect models are based either on a ladder circuit [11] or a parallel-*RL* topology [12]. Both models were originally developed for wires with circular cross section and are inadequate for on-chip applications. We developed a skin effect model based on the direct synthesis of a transfer function for the wire impedance [13]. The transfer function can be directly implemented in the VPEC model, or synthesized as an *RL* equivalent circuit for inclusion in a PEEC framework. Figure 5 shows a comparison between the new skin effect model and FastHenry results. With respect to previous works, the new model accounts for a wide range of the wire aspect ratios, and can be easily tailored to fit numer-

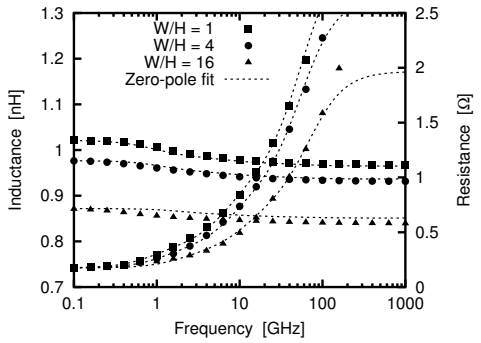

Figure 5: Comparison between FastHenry results (symbols) and the new model based on the direct zero-pole synthesis (dashed lines). Three zero-poles pairs were employed.

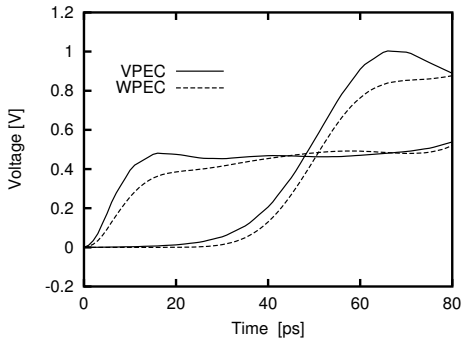

Figure 6: Transient simulation of a 5-mm transmission line, composed of two parallel wires with open-circuit termination. The wave propagation equivalent circuit (WPEC) is compared to VPEC, showing the elimination of the slow rising edge before the time of flight (30 ps).

ical results over any given frequency range.

6 Wave propagation equivalent circuit

Since the VPEC topology is derived from the equations of magnetostatics, wave propagation effects can be accounted for by including the displacement current term in the equations. The resulting wave propagation equivalent circuit (WPEC) promises to unify for the first time transmission line, magnetostatic, and electromagnetic models. Figure 6 shows the application of the new model to the simulation of a simple differential transmission line, comparing WPEC to VPEC models. It is apparent that the improved model, including time-of-flight of the traveling waves, removes the unphysical rising edge before the arrival of the signal at the end of the line.

7 Conclusions

We have reviewed the foundations of the VPEC inductance modeling methodology, discussing several key issues for large-scale and high-frequency CAD applications. Future work will address the full integration of the VPEC model with electromagnetic simulation, which is key to system performance prediction in the multi-gigahertz range.

REFERENCES

[1] M. W. Beattie and L. T. Pileggi, "Inductance 101: Modeling and extraction," in *Proc. Design Automation Conference*, 2001, pp. 323–328.

[2] A. Devgan, H. Ji, and W. Dai, "How to efficiently capture on-chip inductance effects: Introducing a new circuit element *K*," in *Proc. IEEE/ACM International Conference on Computer Aided Design*, 2000, pp. 150 –155.

[3] A. Pacelli, "A local circuit topology for inductive parasitics," in *Proc. International Conference on Computer Aided Design*, San Jose, CA, Nov. 2002, pp. 208–214.

[4] A. Pacelli, P. Wang, and B. Mukherjee, "Vector potential equivalent circuit (VPEC) for PEEC model reduction," submitted to *IEEE Trans. Computer Aided Design*.

[5] H. Yu and L. He, "Vector potential equivalent circuit based on PEEC inversion," in *Proc. Design Automation Conference*, 2003, pp. 718–723.

[6] M. Kamon, M. Tsuk, and J. White, "FASTHENRY: A multipole accelerated 3-D inductance extraction program," *IEEE Trans. Microwave Theory and Techniques*, vol. 42, no. 9, pp. 1750–1758, Sept. 1994.

[7] A. Pacelli, M. Mastrapasqua, and S. Luryi, "Generation of equivalent circuits from physics-based device simulation," *IEEE Trans. Computer Aided Design of Integrated Circuits*, vol. 19, no. 11, pp. 1241–1250, Nov. 2000.

[8] P. M. Xiao, E. Charbon, A. Sangiovanni-Vincentelli, T. Van Duzer, and S. R. Whiteley, "INDEX: an inductance extractor for superconducting circuits," *IEEE Trans. Applied Superconductivity*, vol. 3, no. 1 part 4, pp. 2629–2632, Mar. 1993.

[9] E. B. Rosa, "The self and mutual inductances of linear conductors," *Bulletin of the Bureau of Standards*, vol. 4, no. 2, pp. 301–344, Jan. 1908.

[10] G. Zhong and C.-K. Koh, "Exact closed form formula for partial mutual inductances of on-chip interconnects," in *Proc. IEEE Inl. Conf. on Computer Design: VLSI in Computers and Processors*, 2002, pp. 428–433.

[11] S. Kim and D. P. Neikirk, "Compact equivalent circuit model for the skin effect," in *IEEE Intl. Microwave Symposium Digest*, 1996, pp. 1815–1818.

[12] B. Sen and R. L. Wheeler, "Skin effects models for transmission line structures using generic SPICE circuit simulators," in *IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, 1998, pp. 128–131.

[13] B. Mukherjee, L. Wang, and A. Pacelli, "A practical approach to modeling skin effect in on-chip interconnects," submitted to the 2004 Great Lakes Symposium on VLSI.