Extraction of Extrinsic Series Resistance in RF CMOS

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ABSTRACT

An analytical approach for parameter extraction for CMOS incorporating substrate effect has been presented. The method is based on small-signal equivalent circuit valid in all region of operation, which uniquely extract extrinsic resistances used to extend the industry standard BSIM3v3 MOSFET model for RF applications. The verification of the model was carried out through the measurements of S-parameters and direct time-domain output voltage for a single device at 2.4 GHz in non-linear mode of operation. A circuit level evaluation of the model was carried out using 0.18µm CMOS amplifier and good results for power gain has been achieved.

Keywords: RF CMOS, parameter extraction, non-linear modeling

1 INTRODUCTION

Parasitic series resistance play an important role for RF circuit design and need to be accurately determined. There are many strategies for parameter extraction reported in the literature for CMOS technologies [1-10]. They utilize either full optimisation [1-3], partial parameter optimisation [4], or extraction assuming device symmetry [5]. Lee [4] provides the basic methodology for bulk CMOS, but ignores the effect of the substrate. Raskin [6] presents a comprehensive method for parameter extraction for SOI technology, whereas, Pengg [7] strategy is restricted to a particular region of transistor operation. The present work gives a full derivation of the relevant small signal parameters including the effect of the substrate. The analysis is valid in all regions of operation and does not pre-suppose any symmetry between source and drain [5].

2 EQUIVALENT CIRCUIT AND ANALYSIS

RF MOSFET equivalent circuit incorporating the extrinsic resistance, R_g, R_d, R_s, and R_{sub} is shown in Fig.1. R_g represents the effective distributed gate electrode resistance of multifingers devices connected in parallel and significantly affects the input admittance, whereas the effect of losses in the substrate is modeled by single resistance R_{sub} [8]. Extrinsic source and drain series resistances R_d and R_s included in BSIM3v3 [11] are treated only as virtual components in the current-voltage expression to account for the DC voltage drop across these resistances and therefore, invisible by the signal in the ac simulation. Therefore, external components for these series resistance and need to be included outside the intrinsic model to accurately describe the device AC impedance [2].

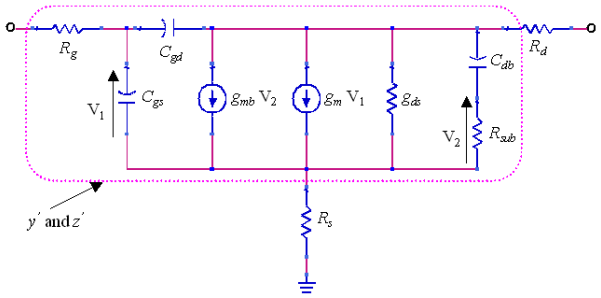


Figure 1: Small-signal equivalent circuit of a MOS transistor valid in all region of operation.

The small-signal circuit shown by dashed part in Fig. 1 can be analysed in terms of y-parameters [12] and the admittance matrix y' is given as

$$y' = \begin{bmatrix} y'_{11} & y'_{12} \\ y'_{21} & y'_{22} \end{bmatrix} \quad (1)$$

$$y'_{11} = \omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega(C_{gs} + C_{gd}),$$
$$y'_{12} = -j\omega C_{gd},\ y'_{21} = g_m - j\omega C_{gd}$$
$$y'_{22} = g_{ds} + \omega^2 C_{db}^2 R_{sub}(1 + g_{mb} R_{sub}) + j\omega(C_{gd} + C_{db} + C_{db} g_{mb} R_{sub}).$$

Equation (1) has been derived subject to the assumptions: a) $\omega R_g (C_{gs} + C_{gd}) << 1$ for admittance parameters y'_{11}, y'_{12} and y'_{21}, and b) $\omega R_{sub} C_{db} << 1$ for y'_{22}.

By inverting the y'-matrix in (1), expanding terms and making appropriate simplifications, we obtain the z'-matrix

$$z' = \begin{bmatrix} z'_{11} & z'_{12} \\ z'_{21} & z'_{22} \end{bmatrix} \quad (2)$$

$$z'_{11} = \frac{(g_{ds} + \omega^2 C_{db}^2 R_{sub} + j\omega(C_{gd} + C_{db})}{(-\omega^2 A + j\omega B)}$$

$$z'_{12} = \frac{j\omega C_{gd}}{(-\omega^2 A + j\omega B)},\ z'_{21} = \frac{-(g_m - j\omega C_{gd})}{(-\omega^2 A + j\omega B)}$$

$$z'_{22} = \frac{\omega^2 R_g (C_{gs} + C_{gd})^2 + j\omega(C_{gs} + C_{gd})}{(-\omega^2 A + j\omega B)}.$$

$$A = C_{gd}C_{gs} + C_{db}(C_{gs} + C_{gd});\ B = g_{ds}(C_{gd} + C_{gs}) + g_m C_{gd}$$

Equation (2) has been simplified by applying the following conditions:

c) $\omega << \frac{1}{\sqrt{R_g(C_{gs} + C_{gd})C_{db}R_{sub}}}$; d) $\omega << \sqrt{\frac{g_{ds}}{C_{db}^2 R_{sub}}}$; and

e) $g_{mb}R_{sub} << 1$.

Assumptions (a) to (d) above are valid up to 10 GHz if the device has small number of fingers and condition (e) is true when the transistor is biased closed to threshold region.

Now, using (2) and incorporating the effect of R_s and R_d, the overall z-parameter of the equivalent circuit shown in Fig. 1 can be expressed as

$$z_{12} = \underbrace{R_s + \frac{BC_{gd}}{\omega^2 A^2 + B^2}}_{\mathrm{Re}(z_{12})} + \underbrace{\frac{-j\omega AC_{gd}}{\omega^2 A^2 + B^2}}_{\mathrm{Im}(z_{12})} \quad (3)$$

and $$\mathrm{Re}(z_{22}) \cong R_s + R_d + \frac{(C_{gs} + C_{gd})B}{\omega^2 A^2 + B^2} \quad (4)$$

3 PARAMETER EXTRACTION

To test the validity of the model, S-parameter measurements were performed on a 0.18μm nMOS transistor, comprising 16 parallel gate fingers of 5μm width. After successful de-embedding [13] capacitances of input/output pads to the ground and associated resistors of the lossy substrate, intrinsic z and y-parameters were obtained from the measurements.

3.1 R_s and R_d

By plotting $\mathrm{Re}(z_{12})$ versus $-\mathrm{Im}(z_{12})/\omega$ and taking y-axis intercept of the best fit line gives R_s because at high frequency $-\mathrm{Im}(z_{12})/\omega$ tends to zero, as shown in Fig. 2(a). In (3) and (4) it is evident that $\mathrm{Re}(z_{12})$ and $\mathrm{Re}(z_{22})$ exhibit the same dependence on frequency [6], hence the slope m of the regression line can be derived as

$$m = \frac{d\,\mathrm{Re}(z_{22})}{d\,\mathrm{Re}(z_{12})} = \frac{(C_{gs} + C_{gd})}{C_{gd}} \quad (5)$$

Similarly, by using (3)-(5) an expression for R_d can be derived from the regression line y-axis intercept c, slope m as shown in Fig. 2(b) and extracted value of R_s as

$$R_d = c + (m-1)R_s \quad (6)$$

It has been suggested that the source/drain resistances become less bias dependent as gate length is reduced to deep sub-micron region [14]. This has been verified through extraction at a number of bias points as shown in Fig. 3, where at low-drain bias, the dependence of all four extracted resistance parameters on V_{gs} is minimal. Therefore, extracted resistance parameters were assumed bias independent and used to extend BSIM3 model [11] for RF applications. Values of $R_s = 2.9\,\Omega$ and $R_d = 6.4\,\Omega$ as obtained from Fig. 2(a) and Fig. 2(b) respectively, have been used for the extraction of rest of the small-signal equivalent circuit parameters.

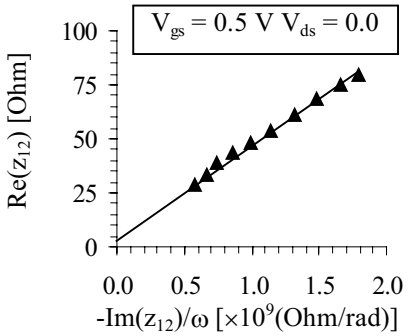


Fig. 2(a)

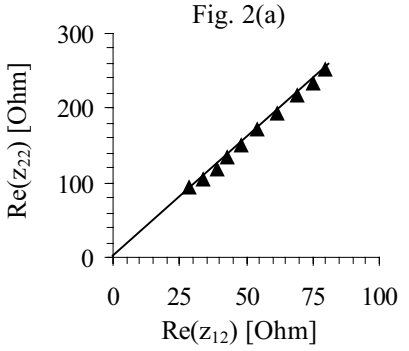


Fig. 2(b)

Figure 2: Extraction of (a) R_s (b) R_d. Measurement frequency 1-10 GHz

3.2 R_g and R_{sub}

Now de-embedding the effect of R_d and R_s in z-parameters domain, each element of the equivalent circuit shown by dashed part in Fig. 1 can be determined in

y-parameters domain [14]. After calculating g_{ds} from $\mathrm{Re}(y_{22}^{'})$ as $\omega \to 0$ and g_{mb} from the non-ideality factor of sub-thresold slope, R_g and R_{sub} can be extracted as

$$R_g = \frac{\mathrm{Re}(y_{11}^{'})}{(\mathrm{Im}(y_{11}^{'}))^2}$$
$$R_{sub} = \frac{\mathrm{Re}(y_{22}^{'}) - g_{ds}}{[\mathrm{Im}(y_{22}^{'}) + \mathrm{Im}(y_{12}^{'})]^2 - g_{mb}[\mathrm{Re}(y_{22}^{'}) - g_{ds}]} \quad (7)$$

Once again, the experimental results in Fig. 3 confirm that R_g and R_{sub} are not strongly bias dependent.

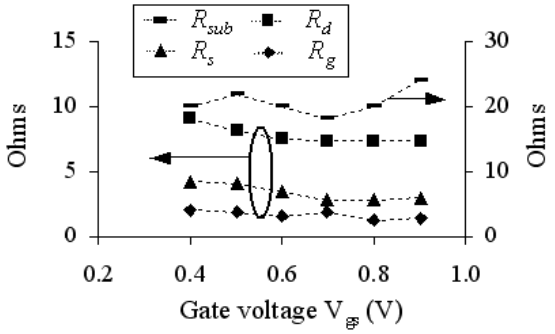


Figure 3: R_g, R_d, R_s and R_{sub} extracted data for $V_d = 0.2V$

4 SIMULATION RESULT

4.1 S-parameters

A comparison of simulation with measurement in Fig. 4 up to a maximum frequency of 10 GHz, shows that S-parameters based on the equivalent circuit fit the measurement even better than the extended BSIM3 model, indicating that all equivalent circuit model parameters are accurately extracted. The addition of R_g R_d improve the prediction S_{11} and S_{21} whereas R_{sub} significantly affect S_{22} at high frequency.

4.2 Time-domain waveform

In Fig. 5 the drain voltage at a frequency of 2.4 GHz is shown at 3 different power levels. It is evident that a better fit in the time domain is obtained at high power when the BSIM3 model is augmented by the four addition series resistences

4.3 Amplifier design

A CMOS amplifier designed using the device sizes shown in Fig. 6 was measured and the BSIM3 based RF model was shown to give good prediction of output power and gain as shown in Fig. 7. Experimental results confirm that the extrinsic resistance parasitics are vital to predict power gain when applied to the CMOS power amplifier.

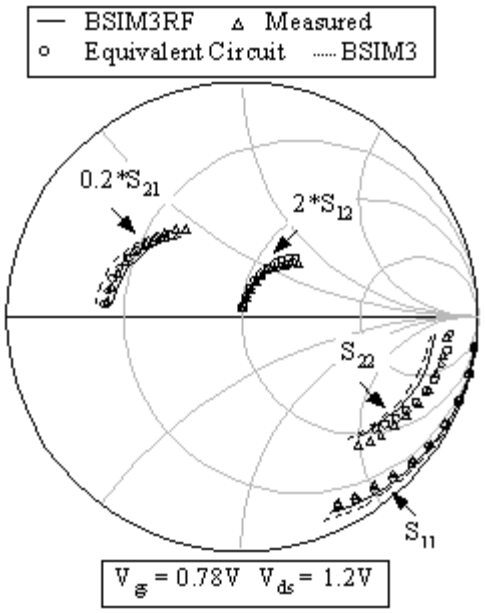
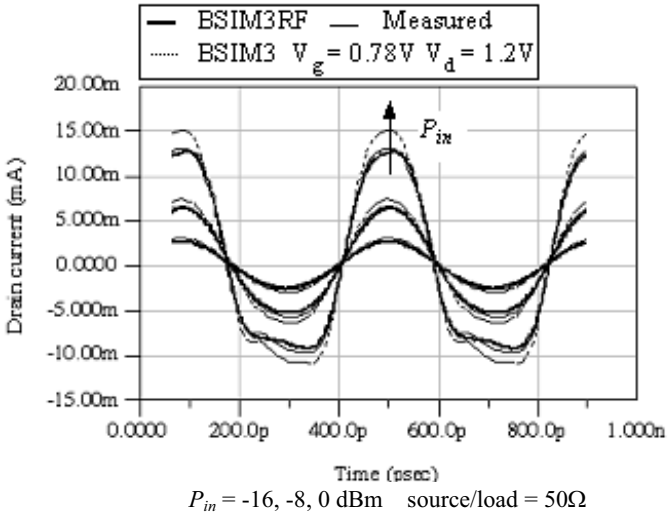


Figure 4: Comparison between the measured, BSIM3RF and equivalent circuit S-parameters



P_{in} = -16, -8, 0 dBm source/load = 50Ω

Figure 5: Time-domain waveform for output drain voltage

5 CONCLUSION

A systematic approach for parameter extraction of extrinsic series resistance for RF CMOS transistor based on a small signal equivalent circuit has been presented. It was found that extraction works well over a wide range of bias conditions and excellent agreement has been achieved between all four simulated and measured S-parameters, indicating that all parameters have been accurately extracted. Adding the extracted resistance to the BSIM3 model gives the opportunity for more accurate non-linear time domain simulation at the device level and harmonic balance (HB) simulation of a CMOS power amplifier at 2.4 GHz

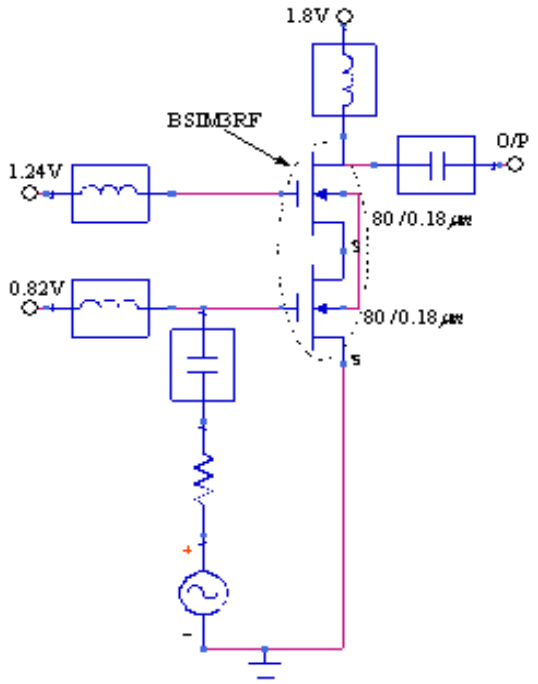


Figure 6: Schematic of CMOS power amplifier

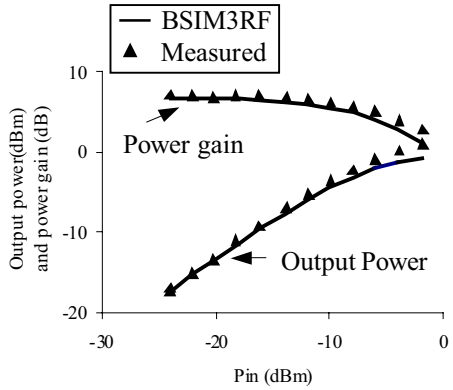


Figure 7: Fundamental power sweep source/load = 50Ω

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